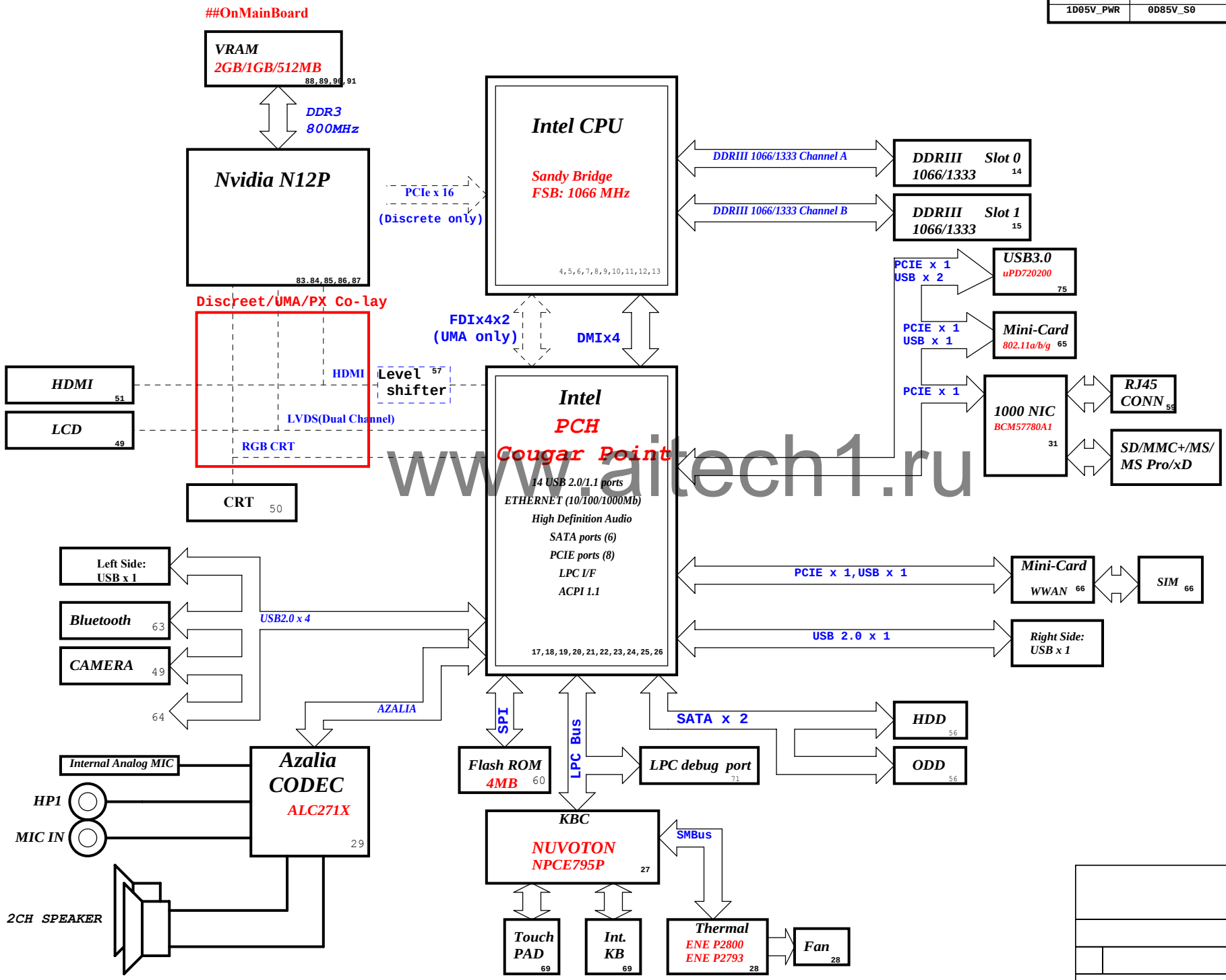

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

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PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.

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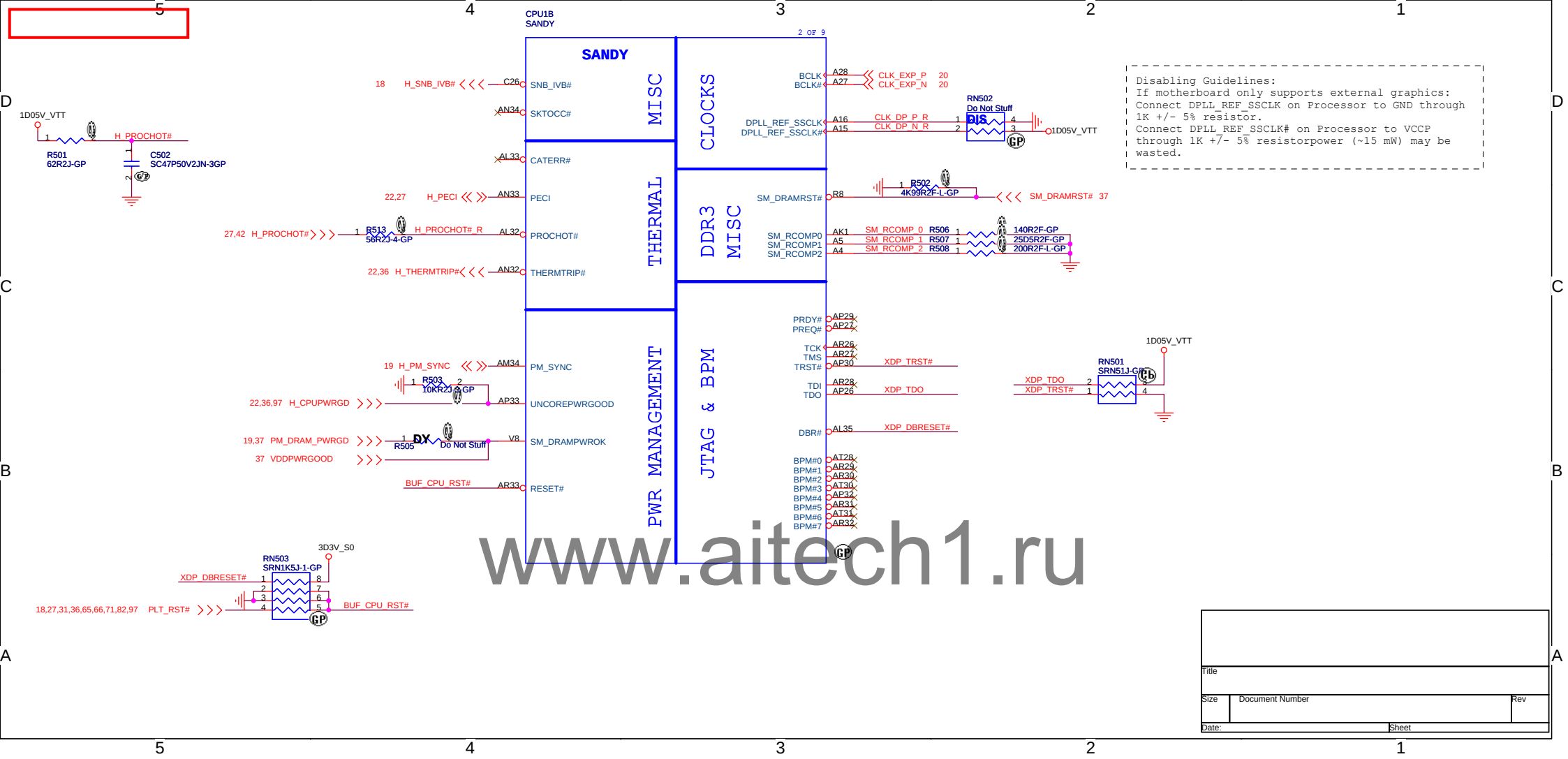

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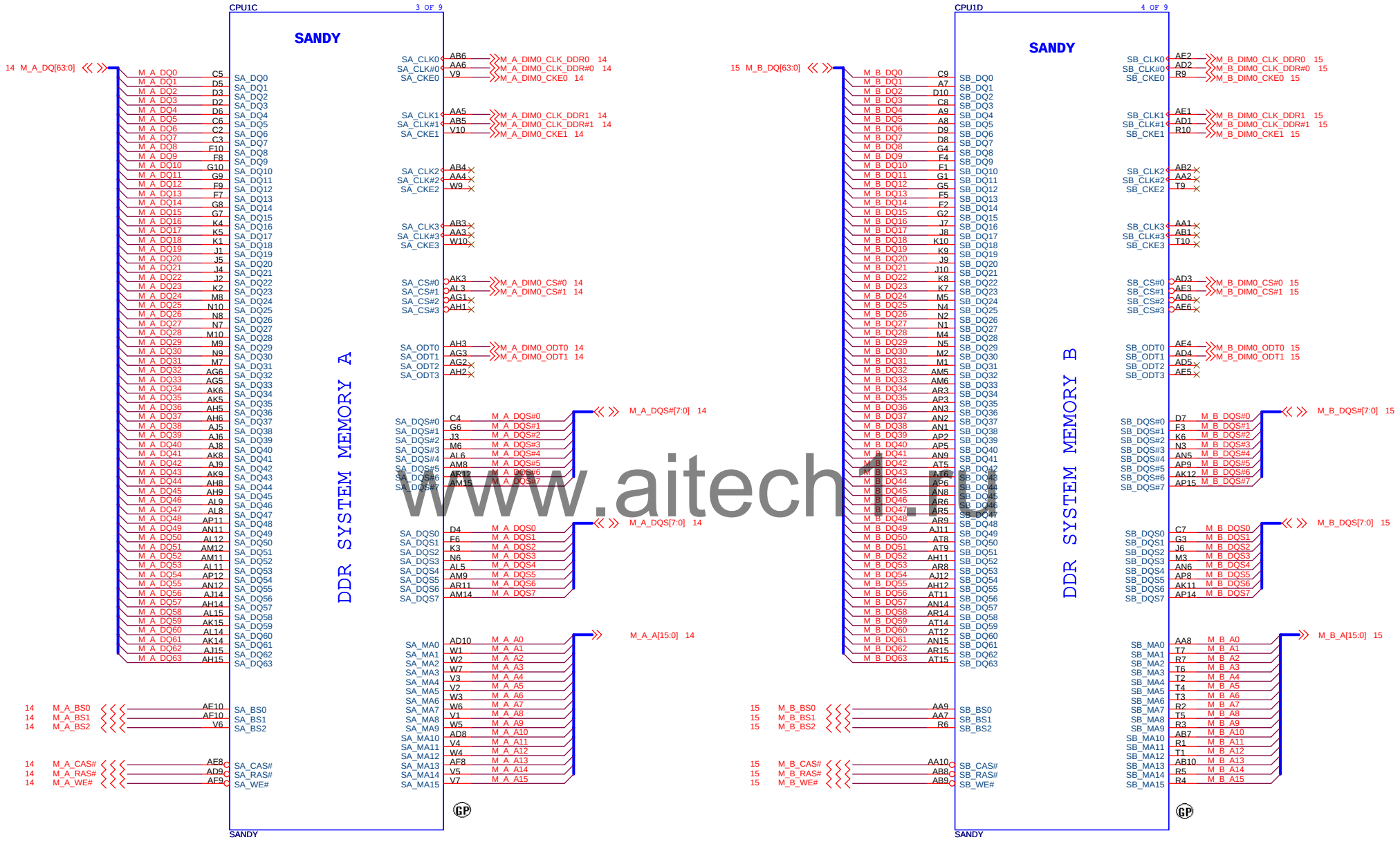

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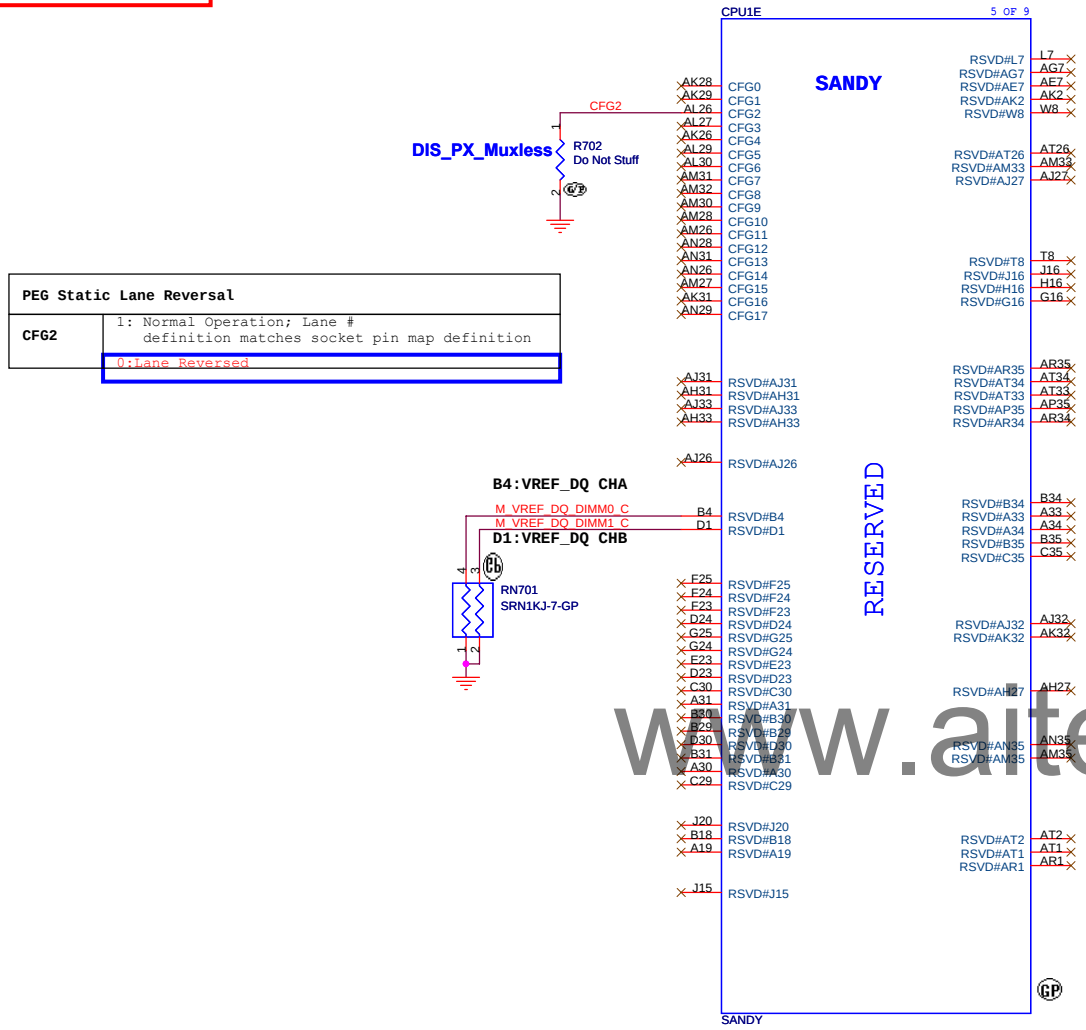

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POWER

6 OF 9

PROCESSOR CORE POWER

53A

CPU1F

SANDY

PEG AND DDR

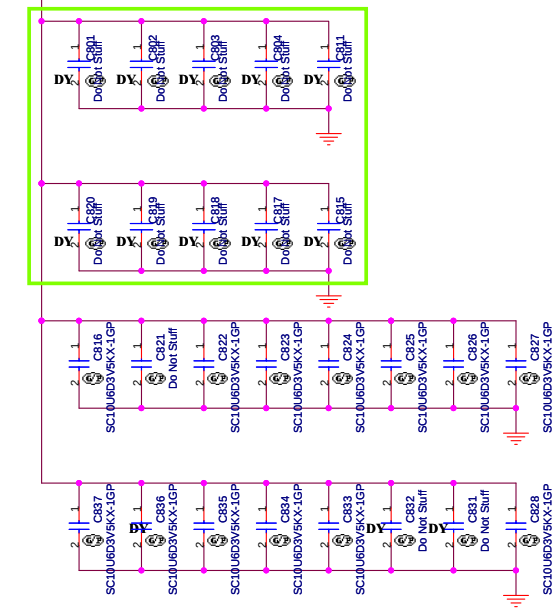
CORE SUPPLY

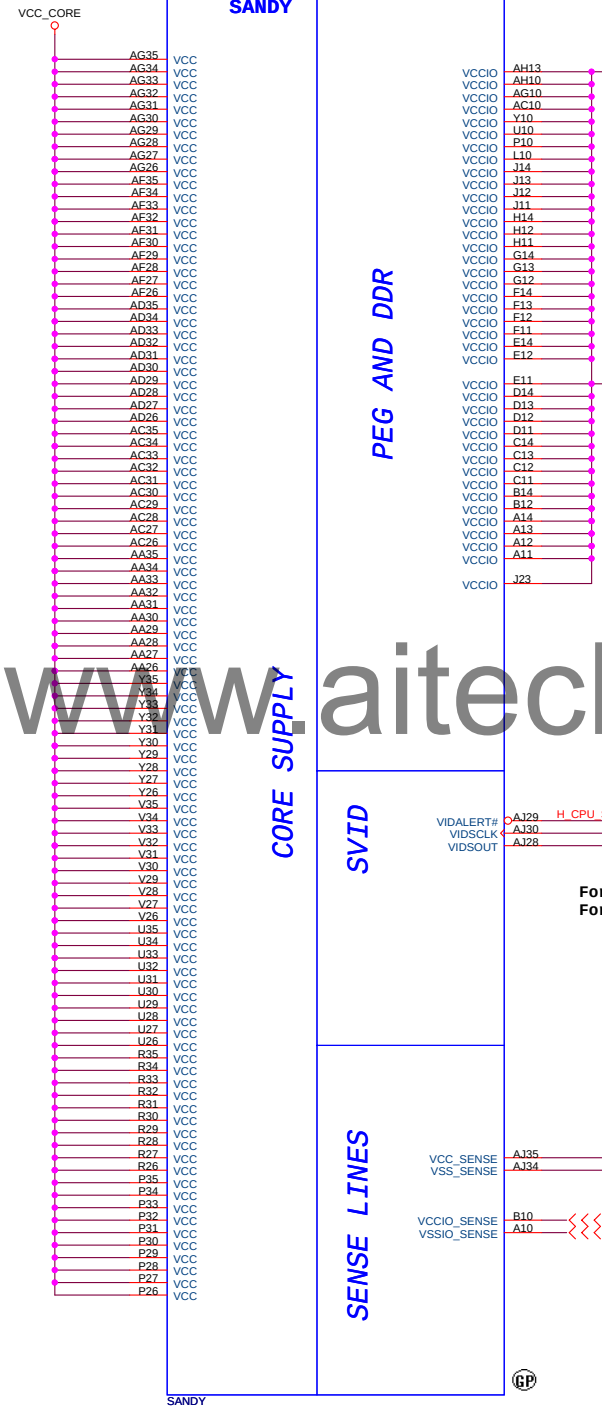
SVID

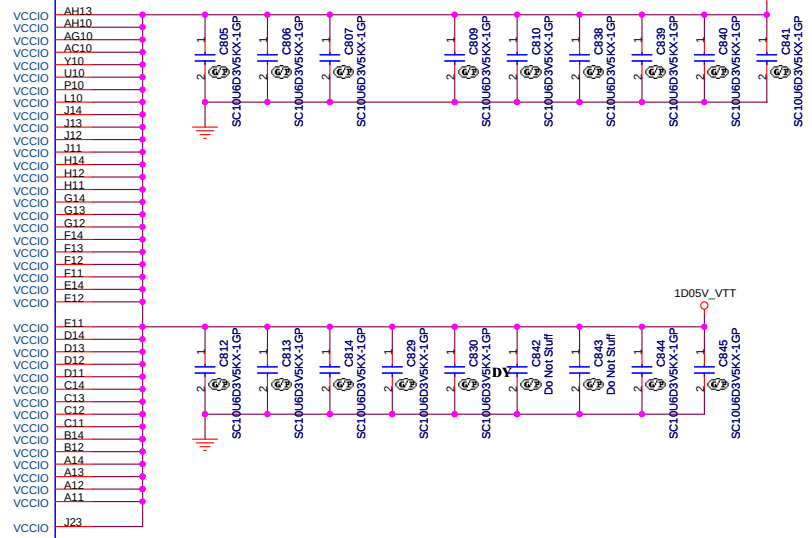
SENSE LINES

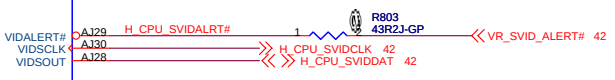
VCC_CORE

1D05V_VTT

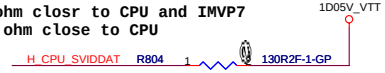


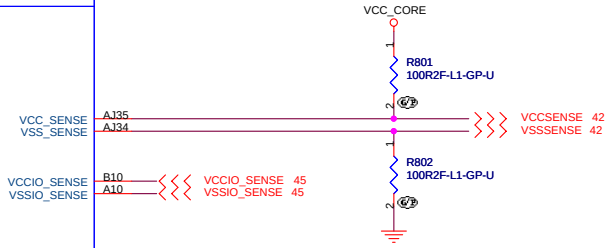






For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU





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VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff DY; C902 SC1U6D3V5KX-1GP; C903 SC1U6D3V5KX-1GP; C904 SC1U6D3V5KX-1GP; C905 SC1U6D3V5KX-1GP; C906 Do Not Stuff DY
UMA_PX_Muxless

C907 Do Not Stuff DY; C908 SC10U6D3V5KX-1GP; C918 Do Not Stuff DY; C919 SC10U6D3V5KX-1GP; C920 SC10U6D3V5KX-1GP; C921 SC10U6D3V5KX-1GP
UMA_PX_Muxless

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

VCC_GFXCORE

R903 Do Not Stuff DIS; R904 Do Not Stuff DIS; R905 Do Not Stuff DIS; R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1
+V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AF7 AF4 AF1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff DY; C910 SC10U6D3V5KX-1GP; C911 SC10U6D3V5KX-1GP; C912 SC10U6D3V5KX-1GP; C913 SC10U6D3V5KX-1GP; C914 Do Not Stuff DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

C916 Do Not Stuff DY; C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0 — R902 10R2J-2-GP — **R902 need be close to pin H23.**

VCCSA_SENSE H23 — VCCUSA_SENSE — TP901 Do Not Stuff

FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6 A6 A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

GRAPHICS

SANDY

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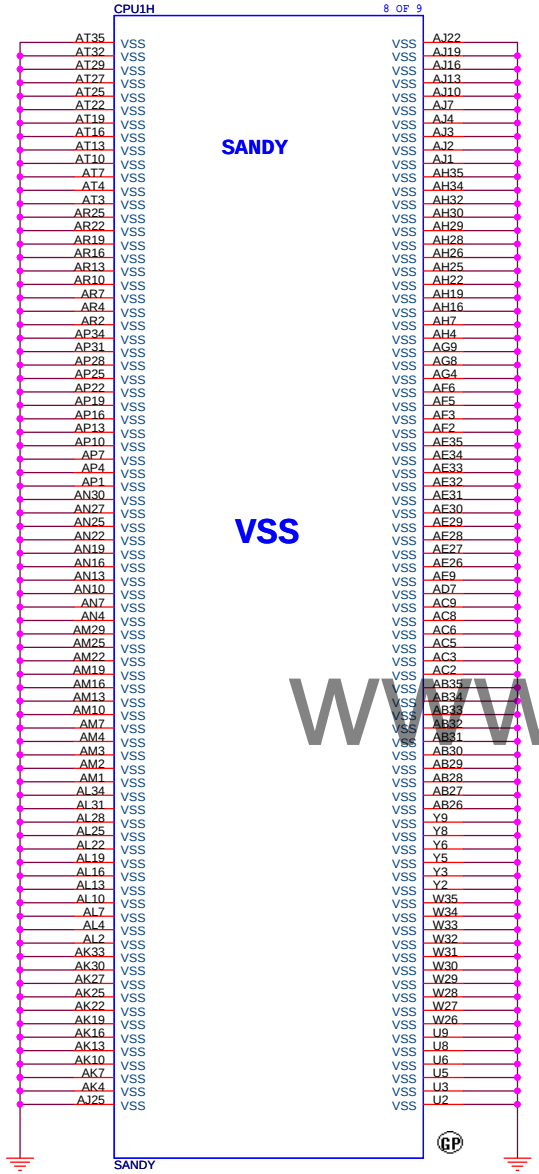

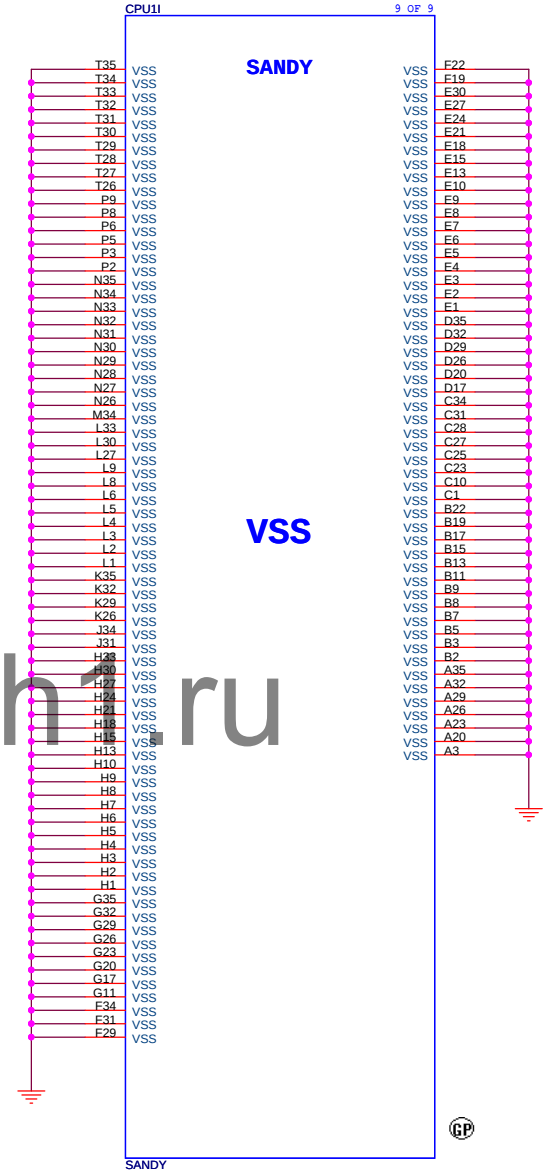

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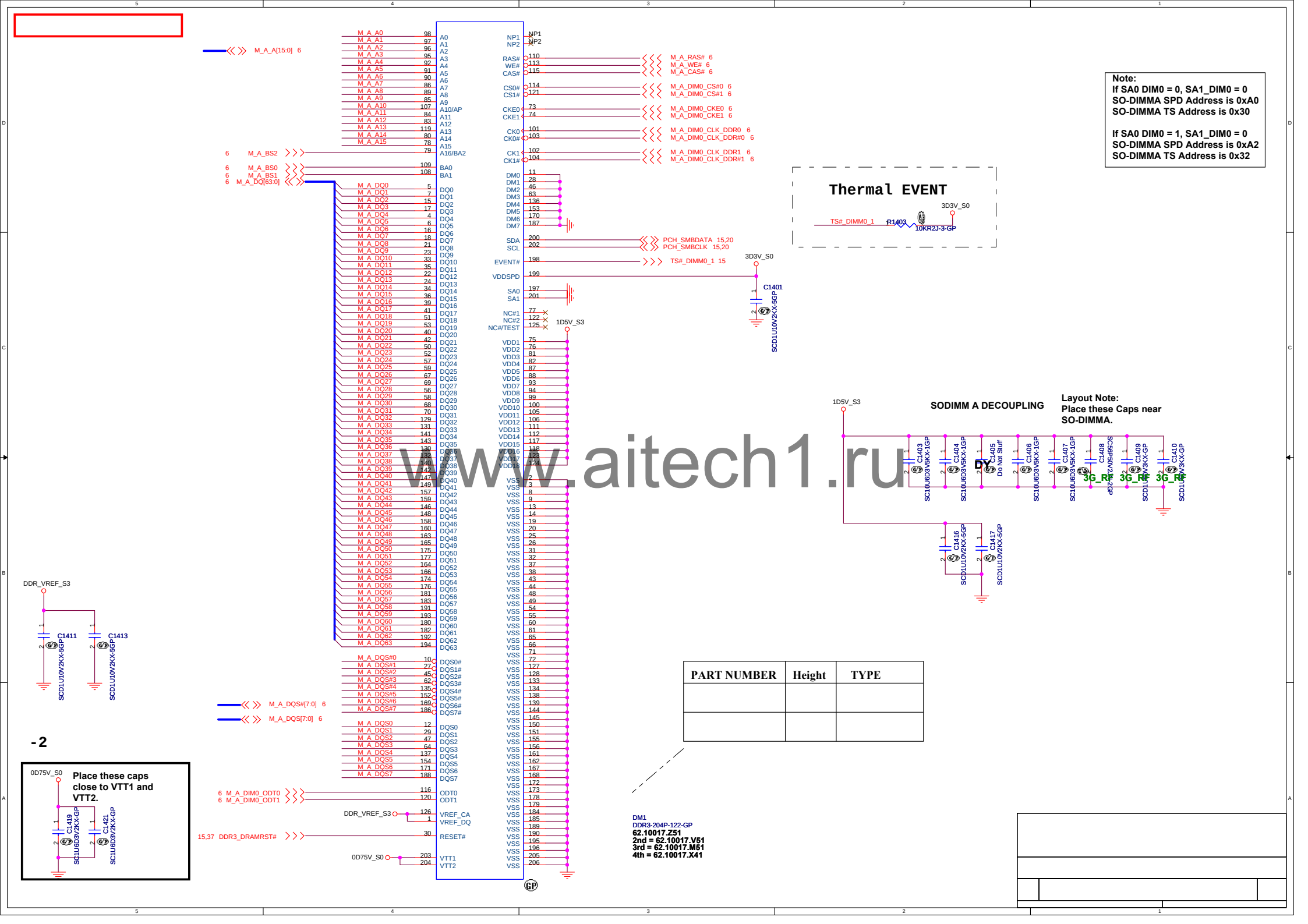

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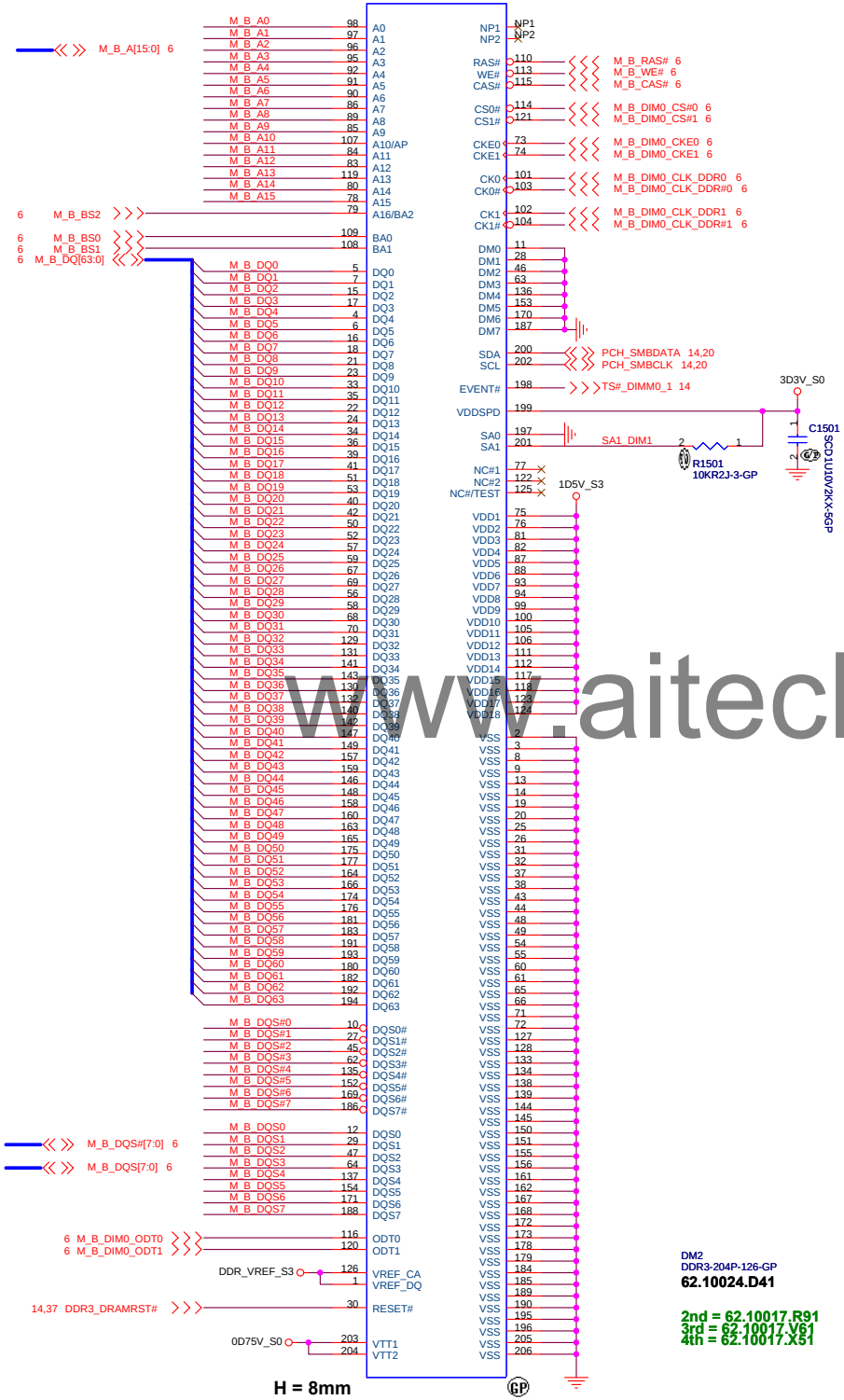
SSID = MEMORY



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DDR_VREF_S3

C1515 SCD1U10V2KX-5GP

C1517 SCD1U10V2KX-5GP

-2

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1519 SC1U6D3V2KX-GP

C1521 SC1U6D3V2KX-GP

H = 8mm

DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

1D5V_S3

SODIMM B DECOUPLING

C1503 SCS5D6P50V2CN-1GP

3G_RF

C1504 SC68P50V2JN-2GP

C1505 SC10U6D3V5KX-1GP

C1506 SC10U6D3V5KX-1GP

C1507 SC10U6D3V5KX-1GP

C1508 SCD1U10V5KX-GP

C1509 SC10U6D3V5KX-1GP

C1510 SC1D1U50V3KX-5GP

C1513 SCD1U10V2KX-5GP

C1514 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMB.

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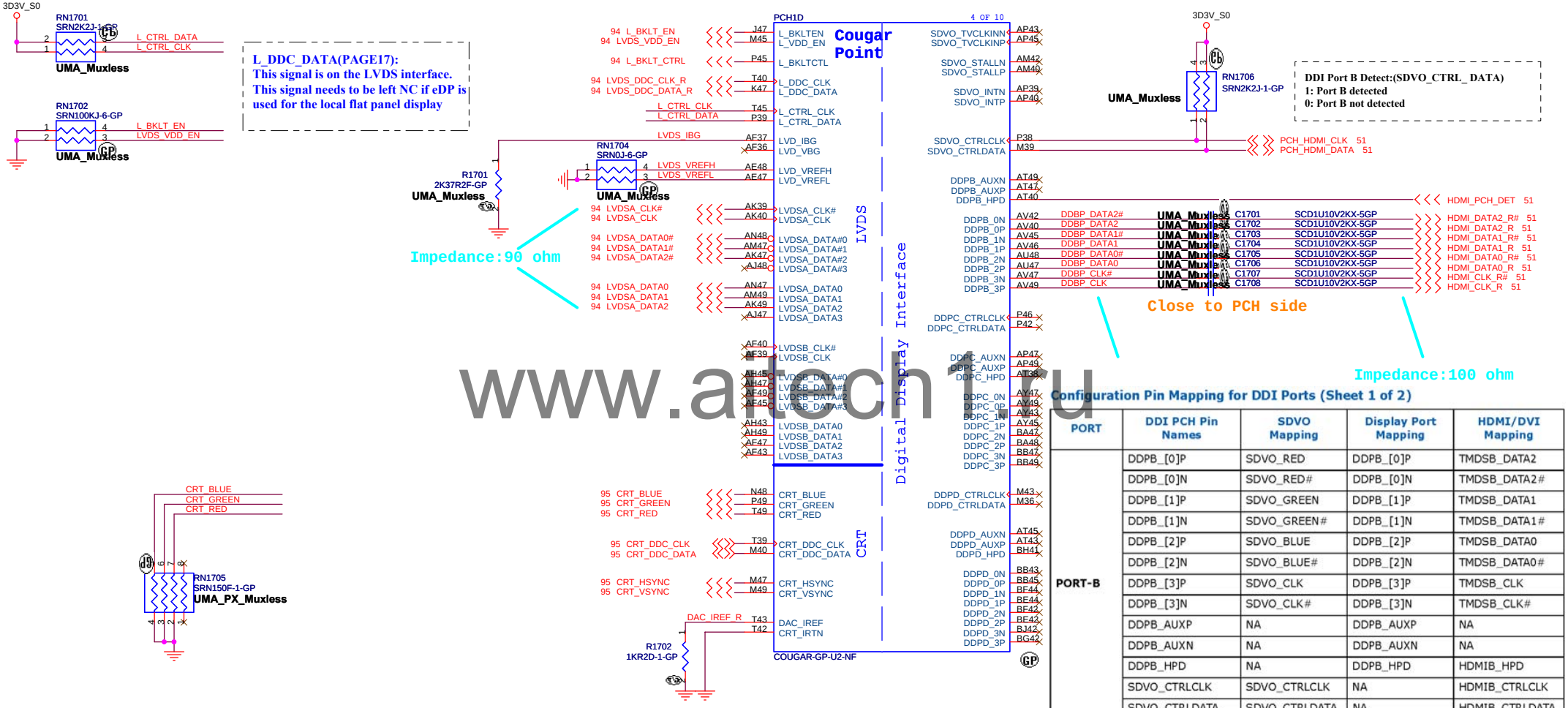

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Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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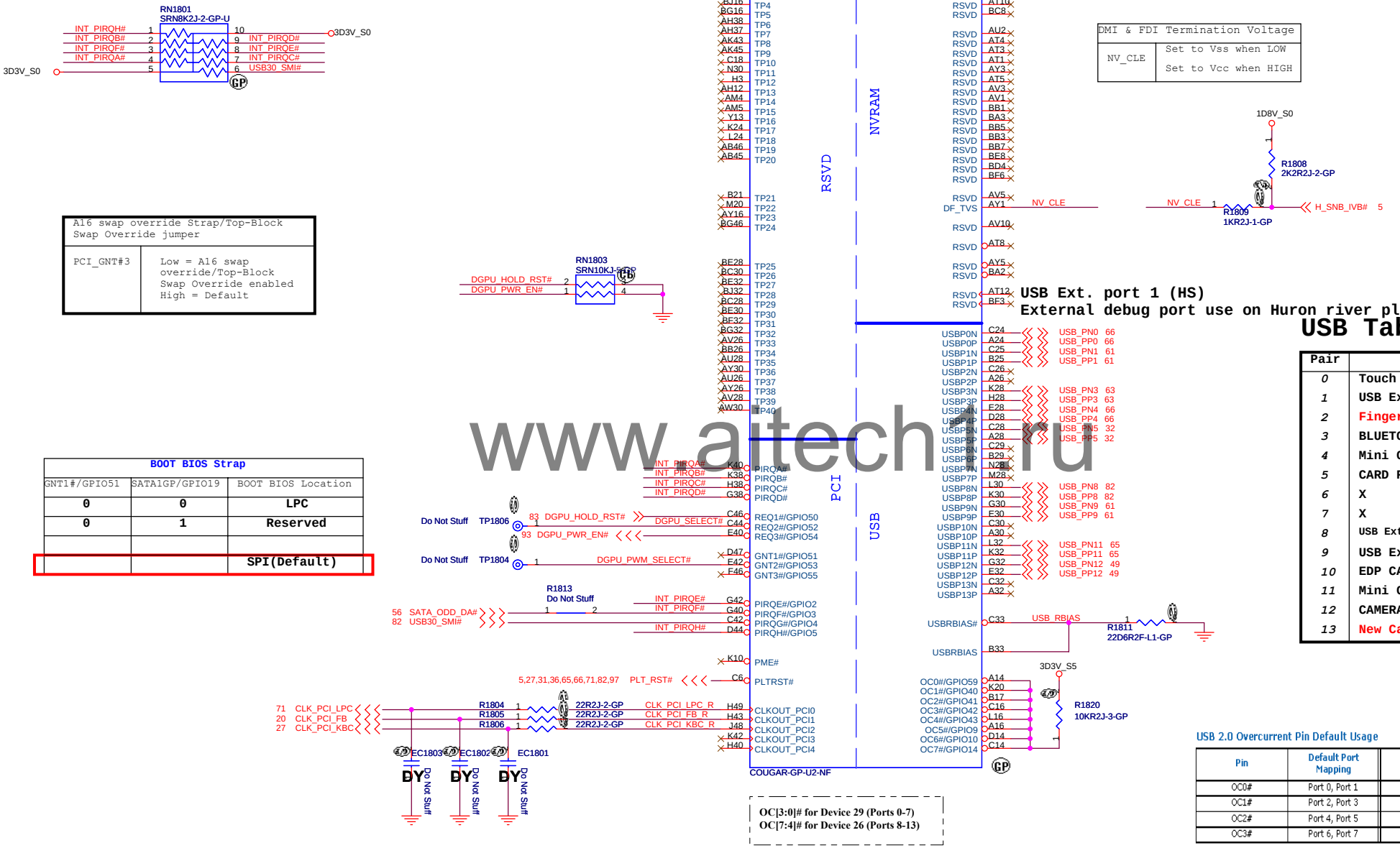
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		SPI(Default)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

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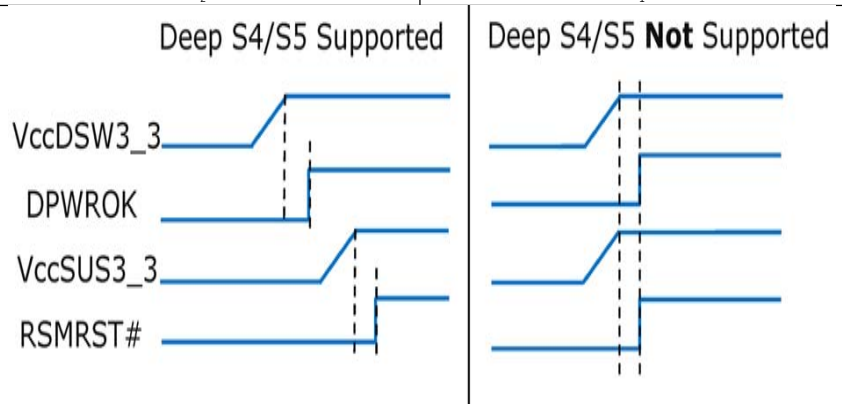
Date: | Sheet

SSID = PCH



PCH1C — Cougar Point — 3 OF 10

DMI: DMI0RXN DMI1RXN DMI2RXN DMI3RXN; DMI0RXP DMI1RXP DMI2RXP DMI3RXP; DMI0TXN DMI1TXN DMI2TXN DMI3TXN; DMI0TXP DMI1TXP DMI2TXP DMI3TXP

FDI: FDI_RXN0-7, FDI_RXP0-7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29

SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

COUGAR-GP-U2-NF

R1901 49D9R2F-GP DMI_COMP_R; R1902 750R2F-GP RBIAS_CPY (1D05V_VTT)

R1926 Do Not Stuff; R1904 100KR2J-1-GP (DY) SYS_PWROK / PWROK

0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.

R1905 10KR2J-3-GP (3D3V_S0) SYS_RESET#

R1924 Do Not Stuff PWROK

R1910 Do Not Stuff; R1911 Do Not Stuff (DY) PM_RSMRST# → RTC_AUX_S5

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

RTC_AUX_S5 — R1917 330KR2J-L1-GP; R1918 Do Not Stuff (DY) — DSWODVREN

R1919 8K2R2J-3-GP (3D3V_S0) PM_CLKRUN#

RN1901 SRN10KJ-6-GP (3D3V_S5): BATLOW#, PM_RI#, AC_PRESENT, SUS_PWR_ACK

R1921 10KR2J-3-GP PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP PM_RSMRST#

3D3V_AUX_S5: R1909 100KR2J-1-GP; R1916 10KR2J-3-GP; 3V_5V_POK_#

Q1901 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

R1912 1KR2J-1-GP PM_RSMRST# → RSMRST#_KBC 27; 3V_5V_POK 41

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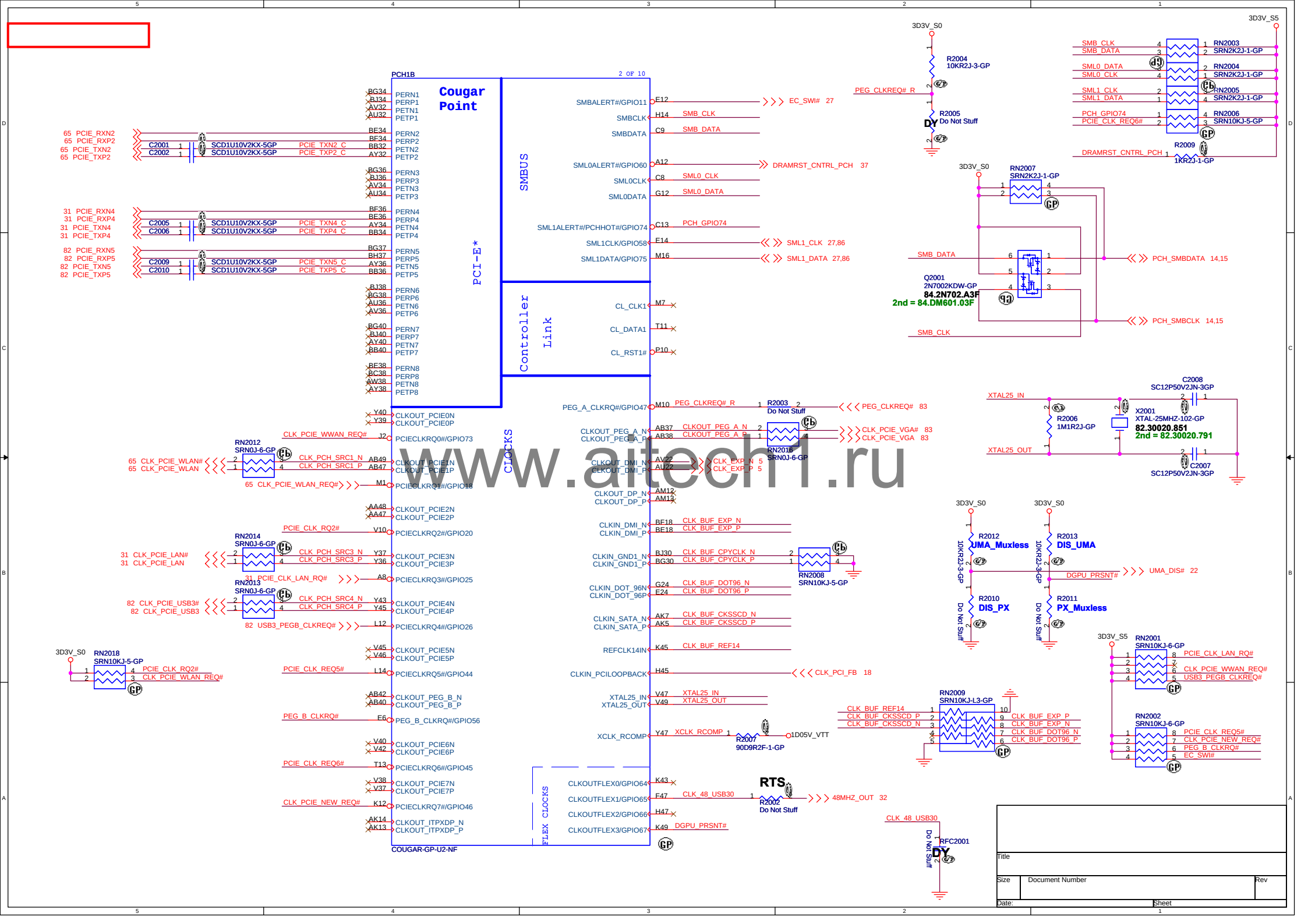

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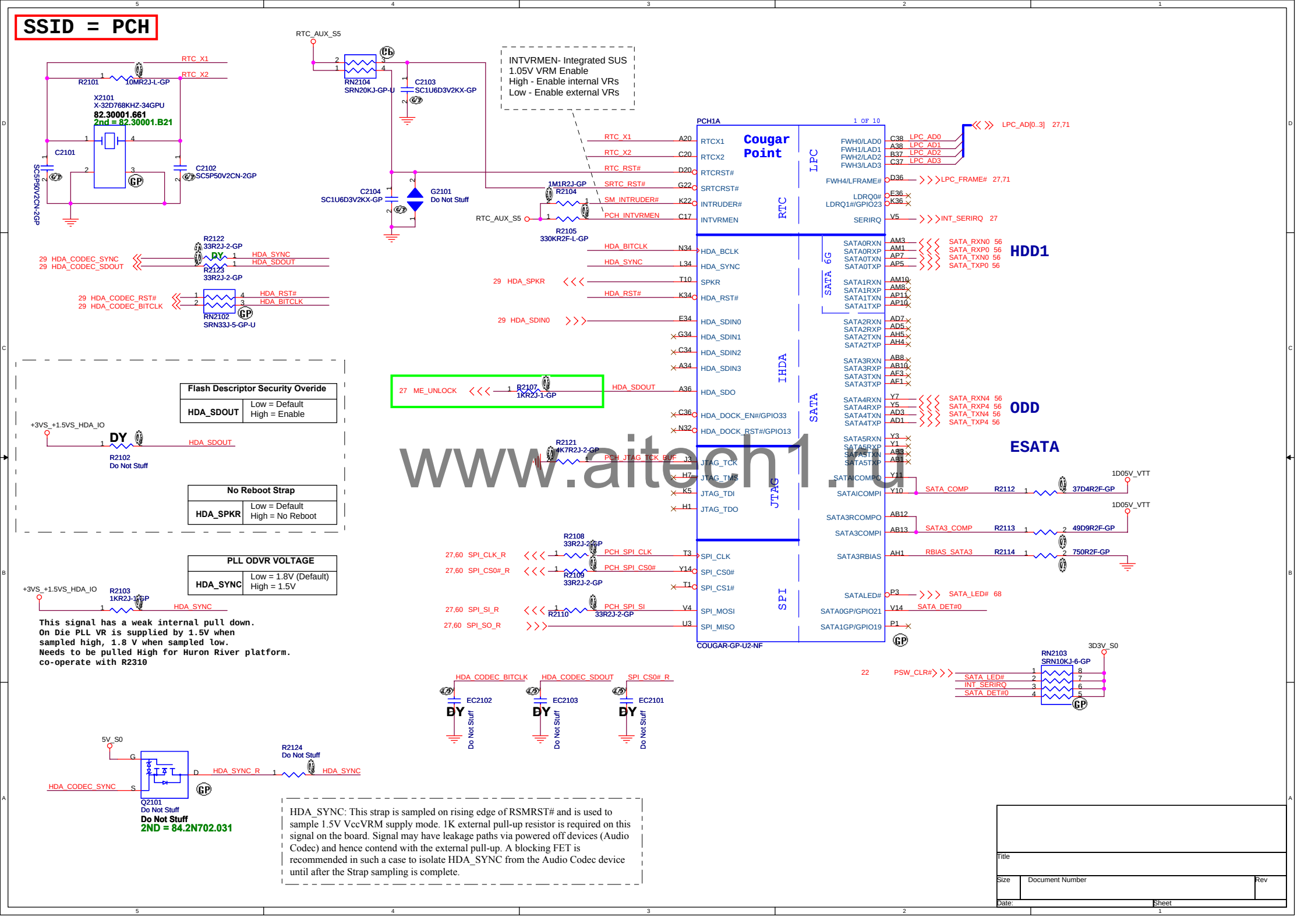
SSID = PCH



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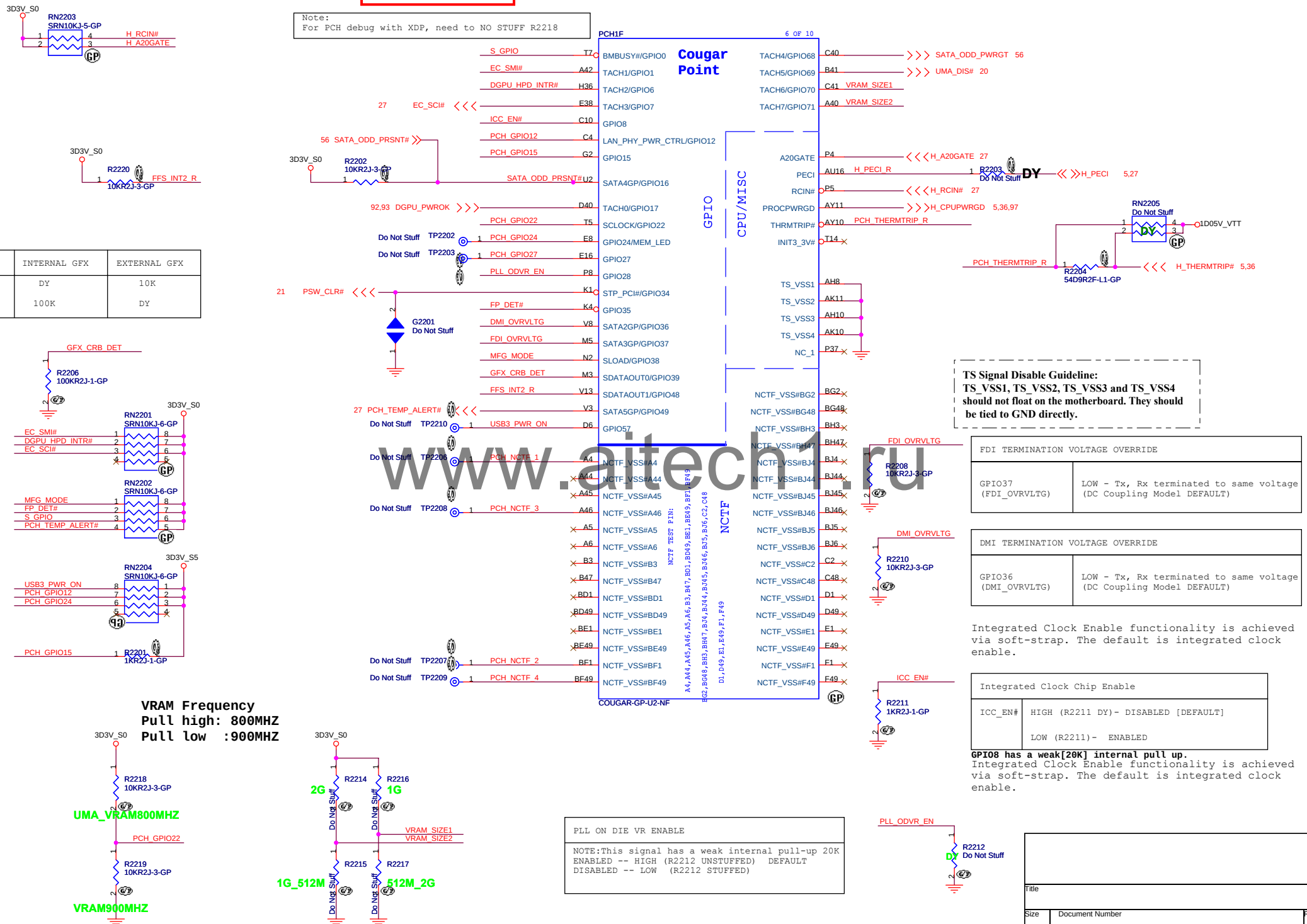

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

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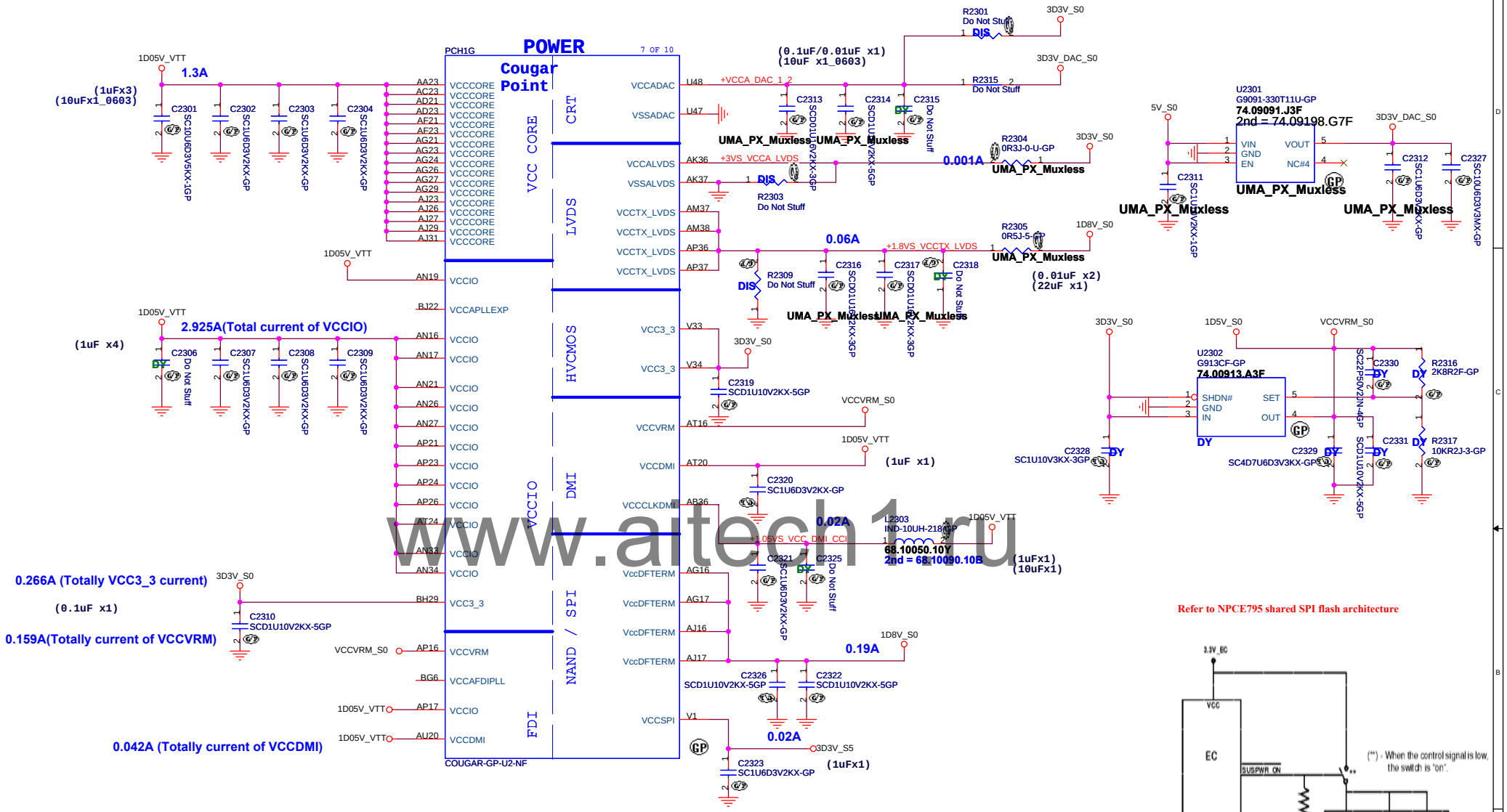
SSID = PCH



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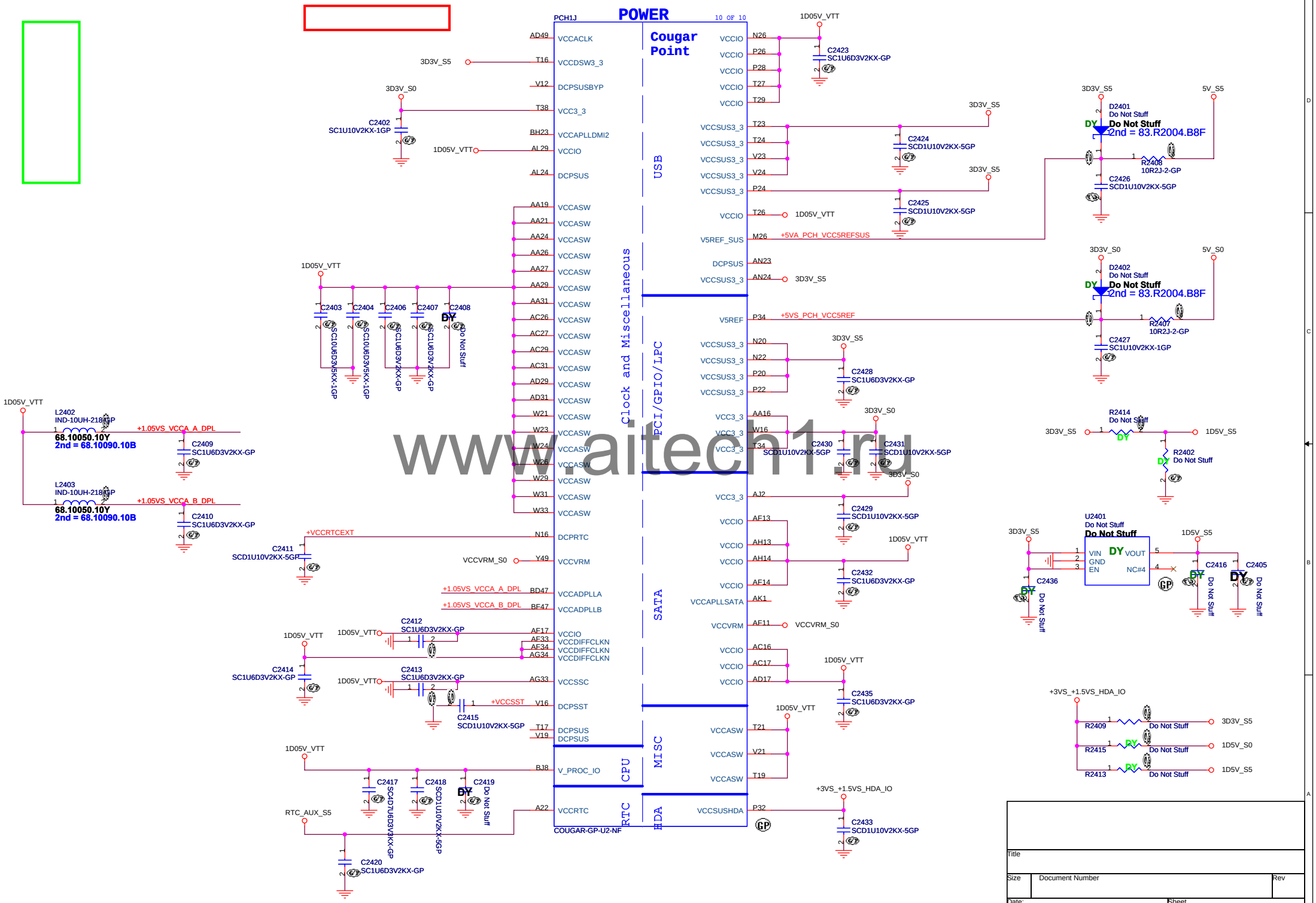

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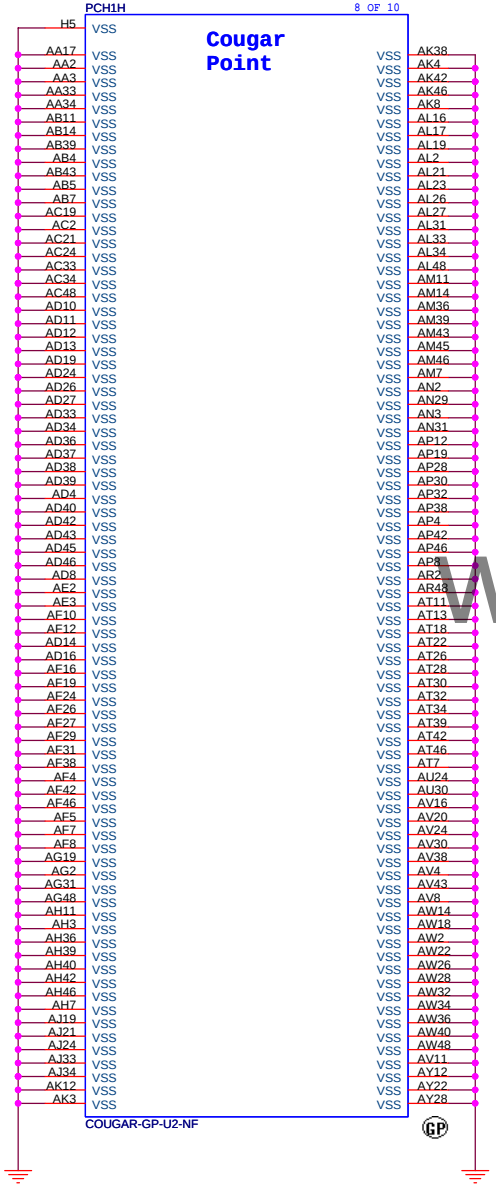

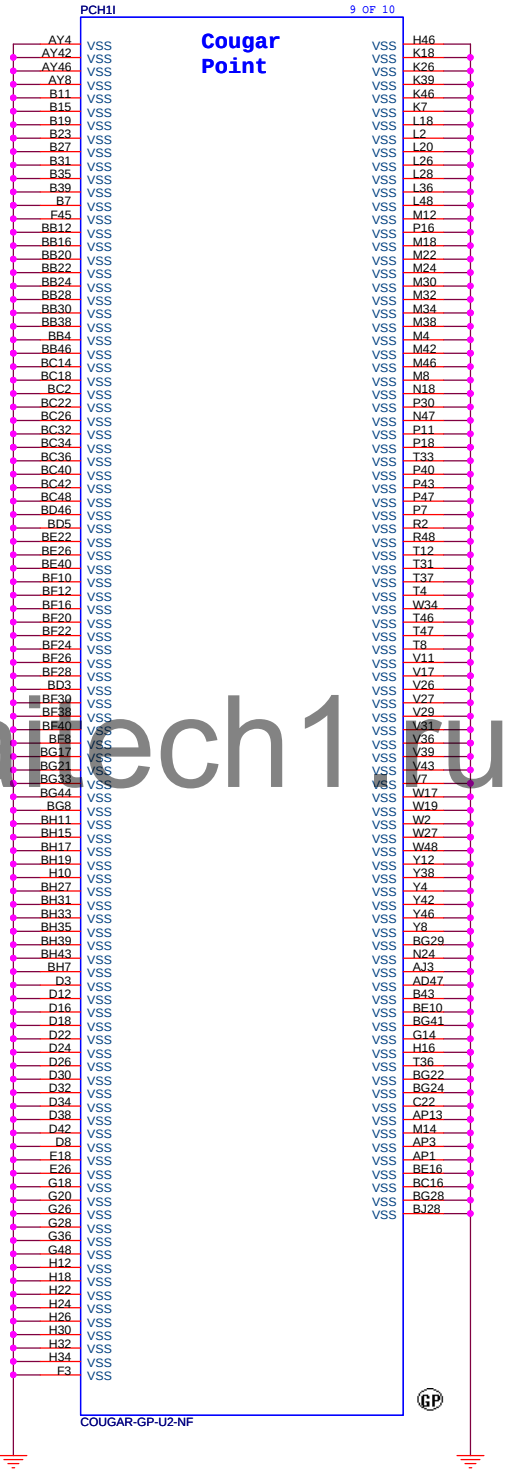

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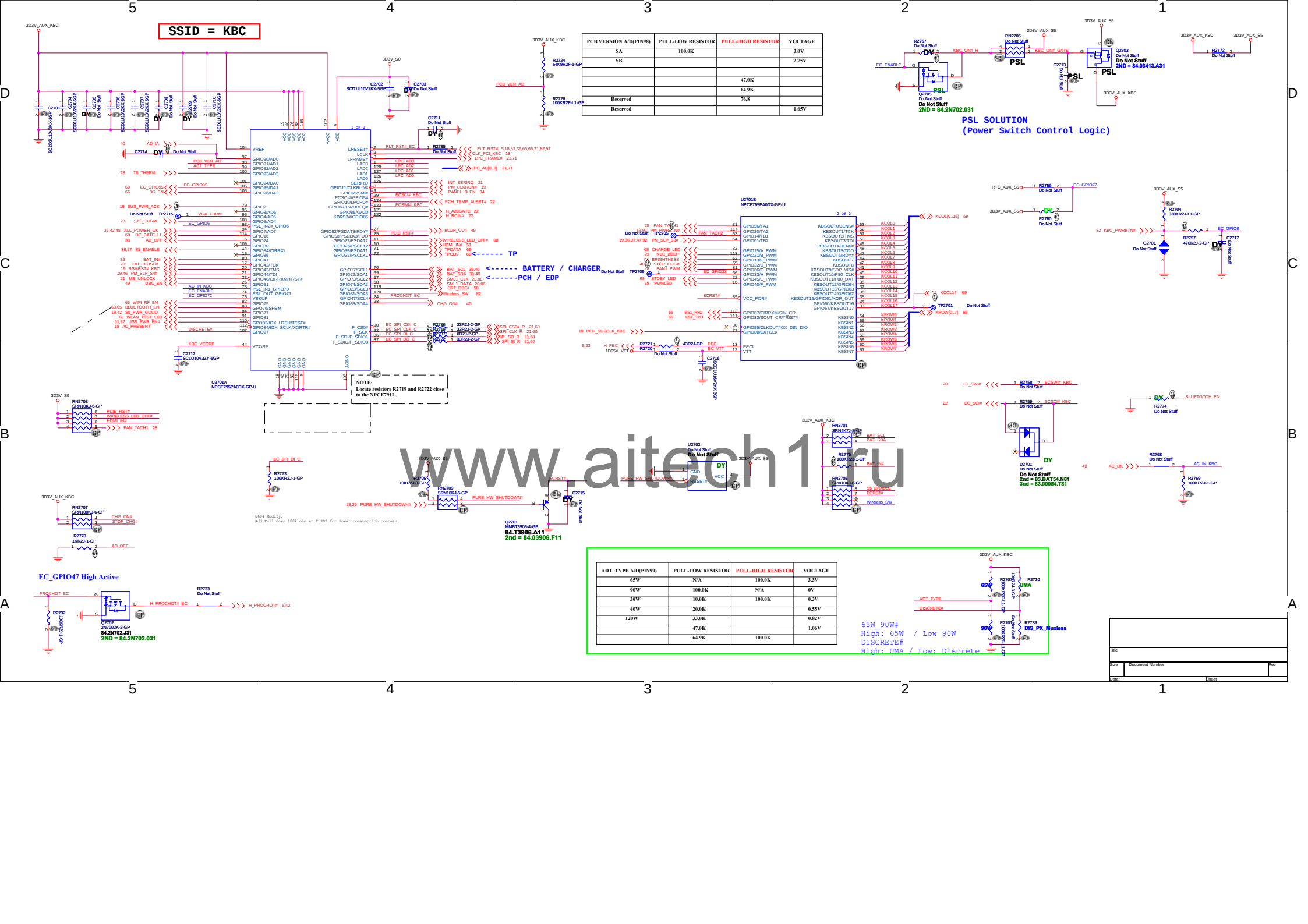
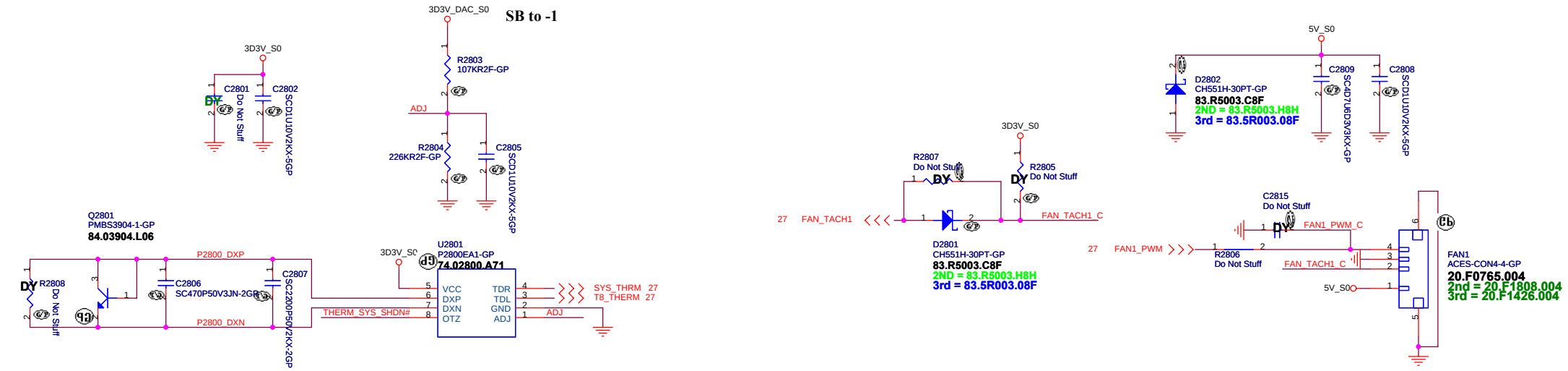


PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K		3.0V
SB			2.75V
		47.0K	
		64.9K	
Reserved		76.8	
Reserved			1.65V

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K		0.55V
120W	33.0K		0.82V
	47.0K		1.06V
	64.9K	100.0K	



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

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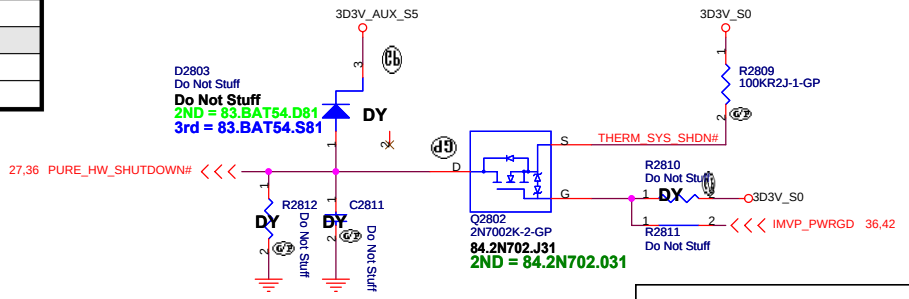

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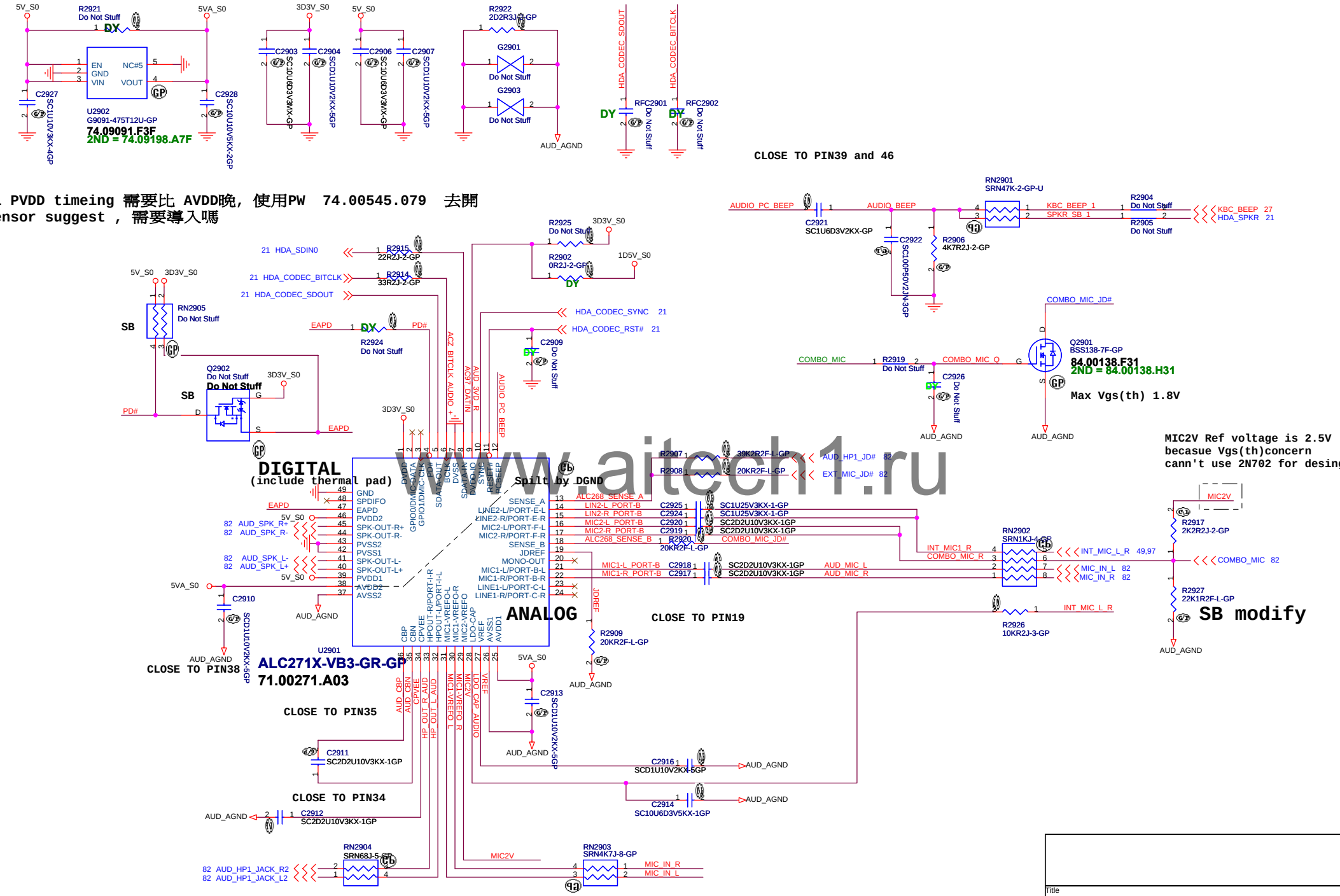
-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN39 and 46
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2902
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V
MIC2V Ref voltage is 2.5V becasue Vgs(th)concern cann't use 2N702 for desing
SB modify
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN19
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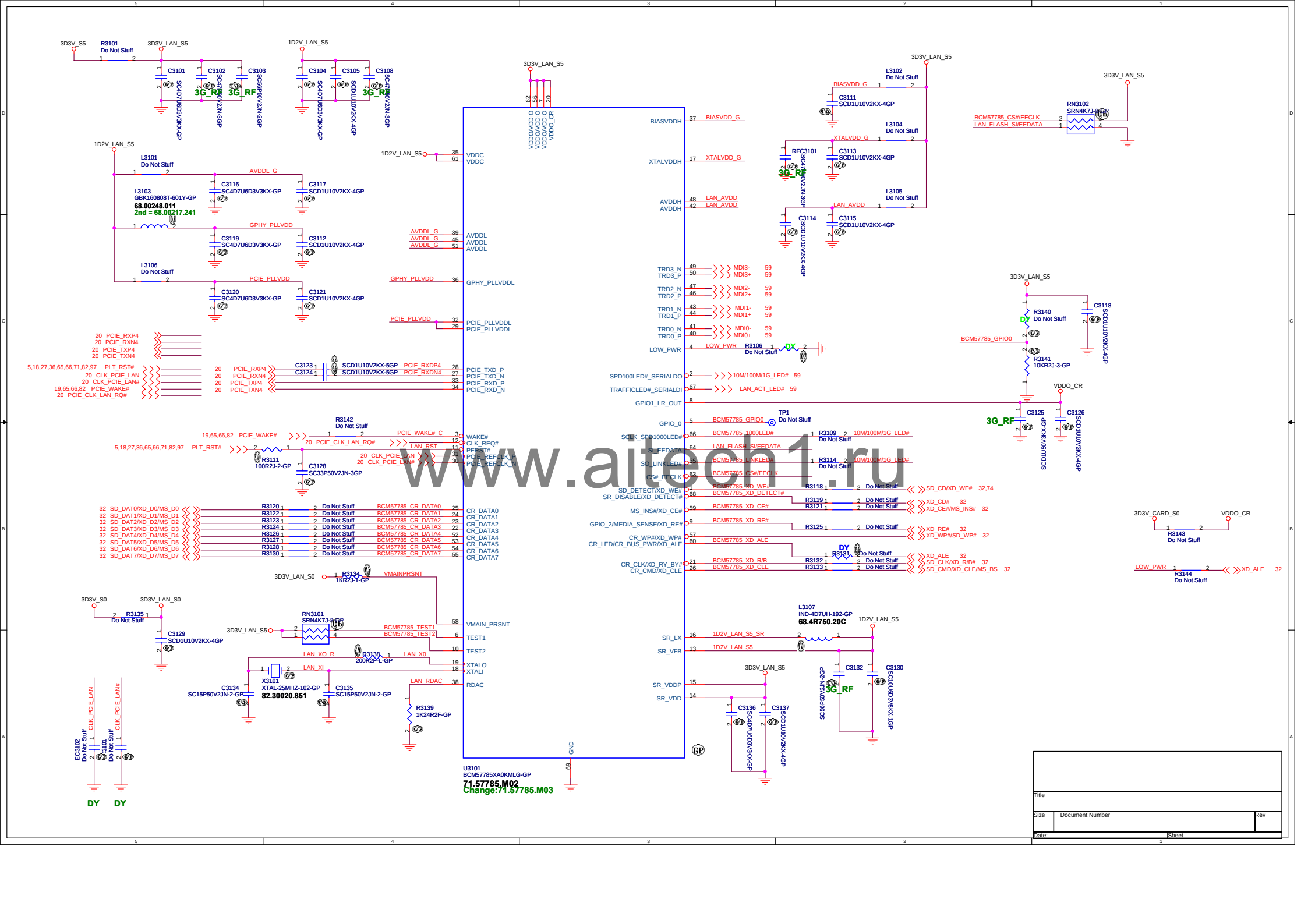
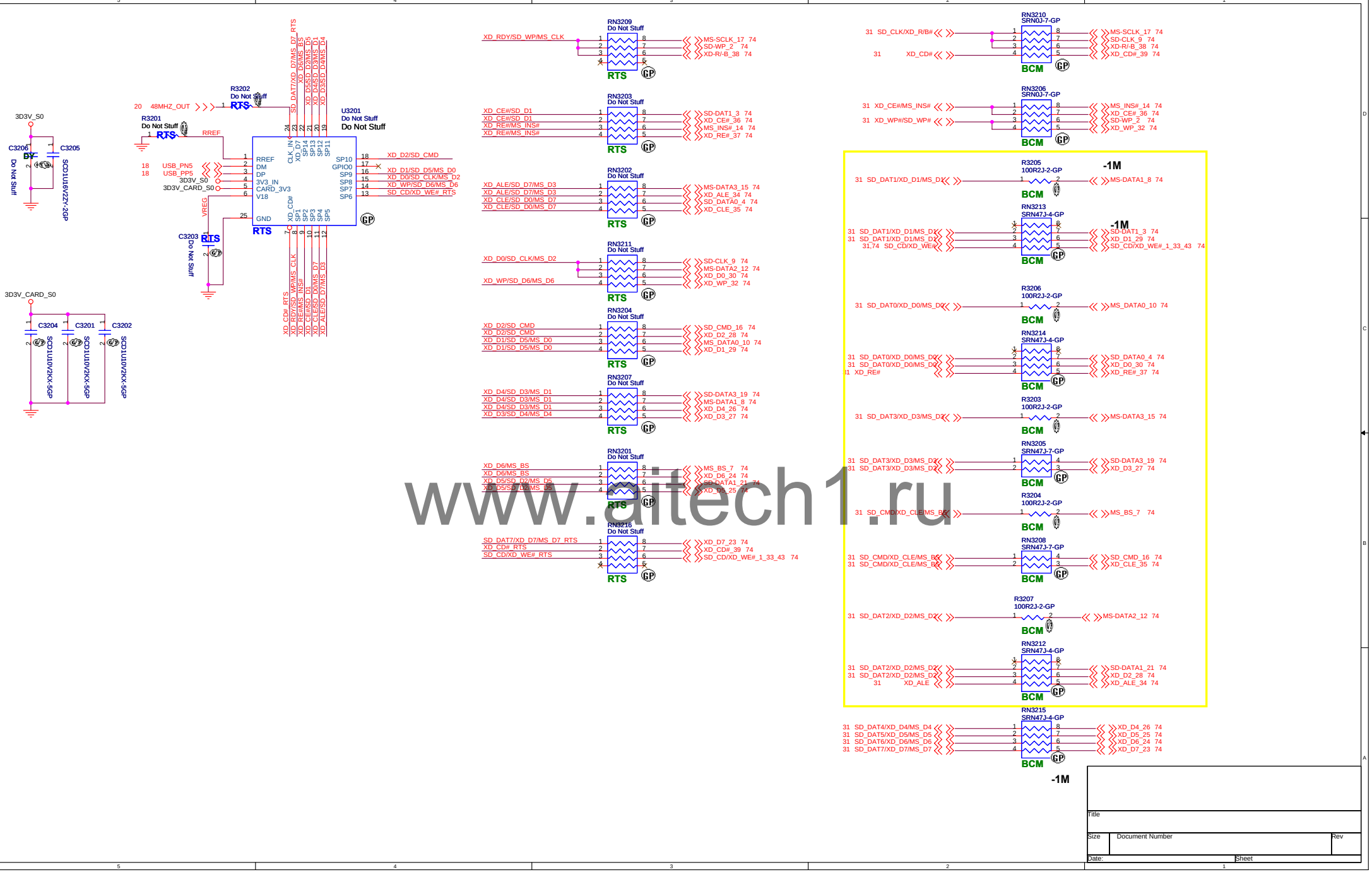


www.aiteen1.ru



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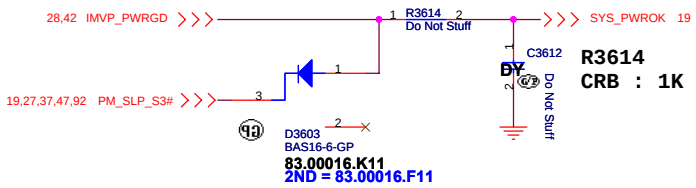
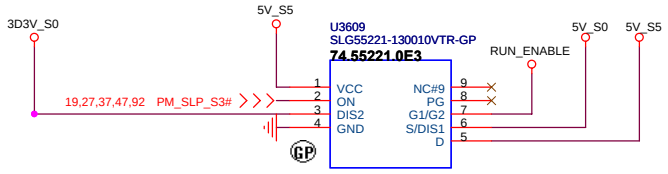
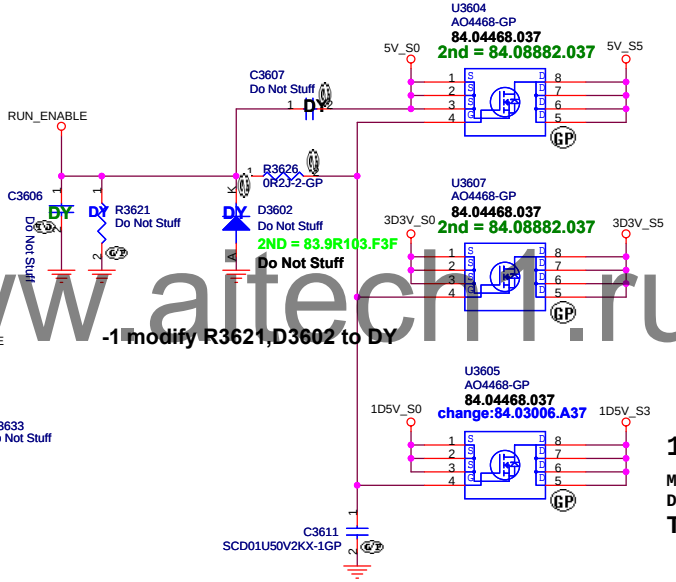
Power Sequence

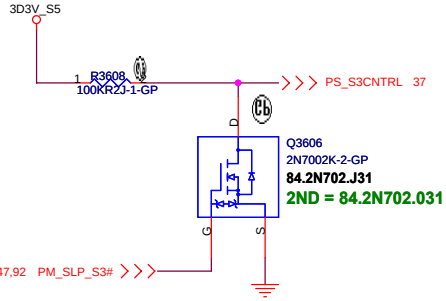


R3614
CRB : 1K

ANNIE Run Power







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-1 modify R3621,D3602 to DY

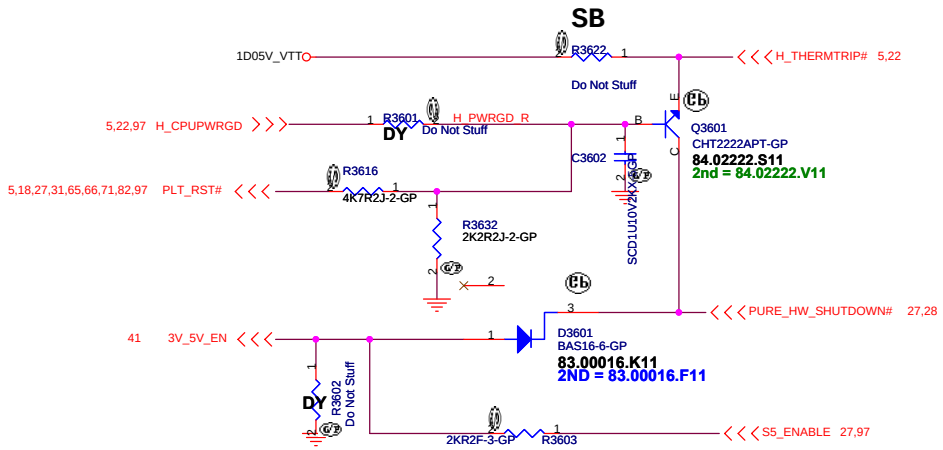
SB modify part number

-1 co-layout SLG55221

1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



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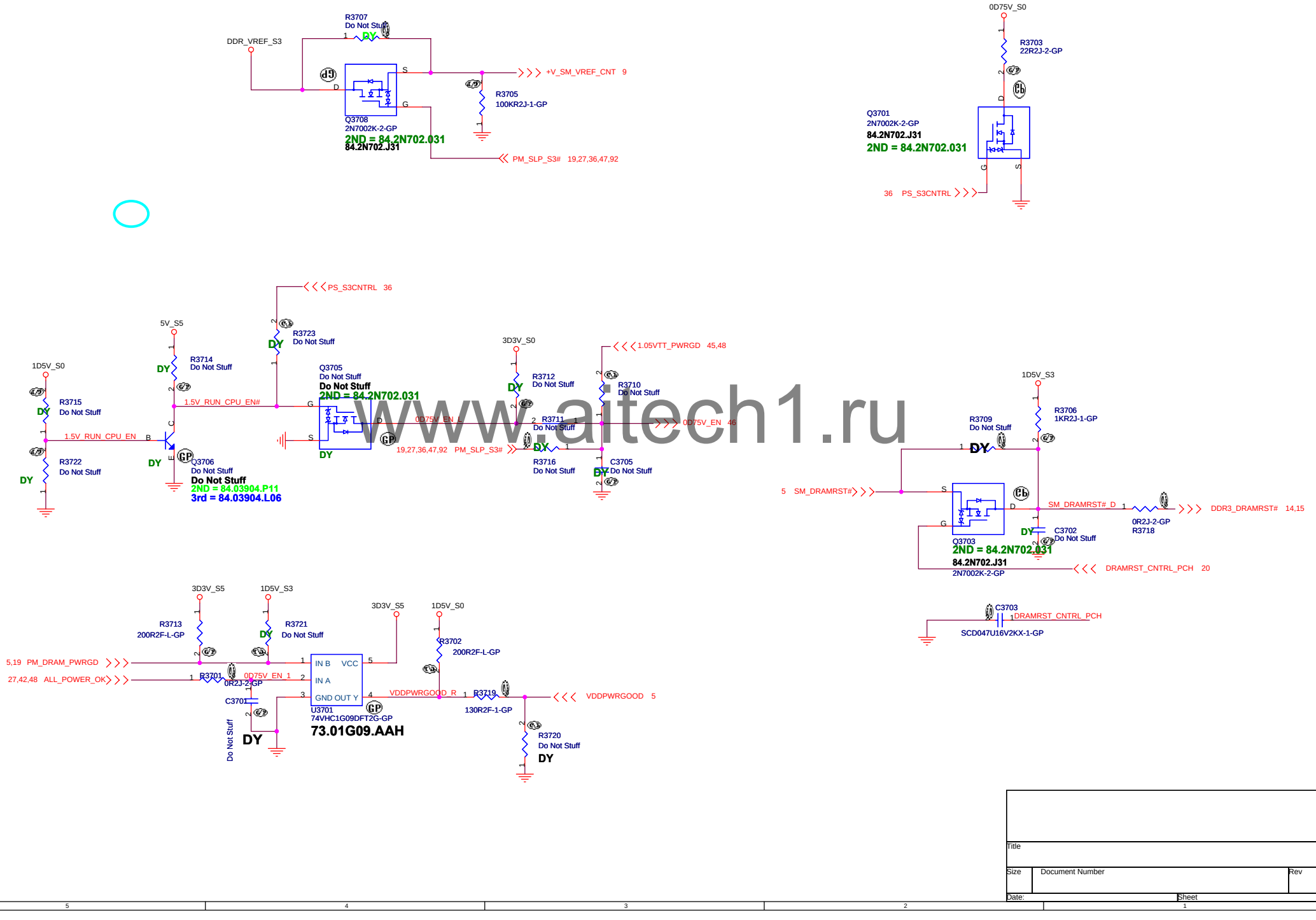

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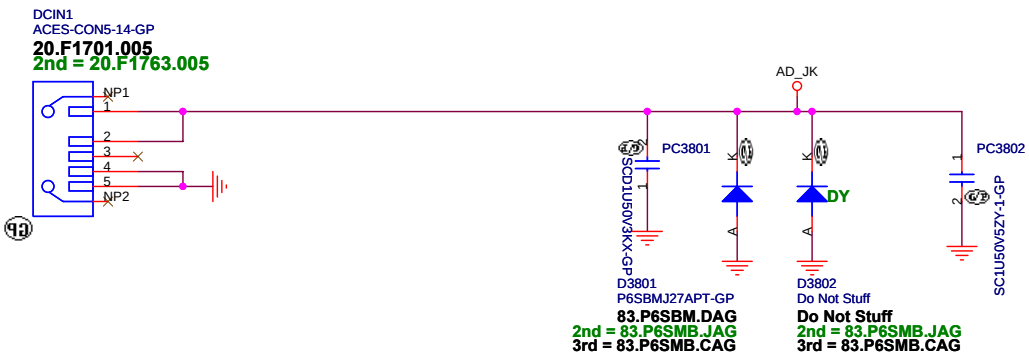

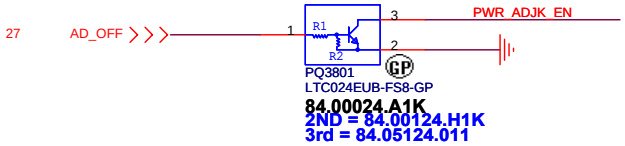

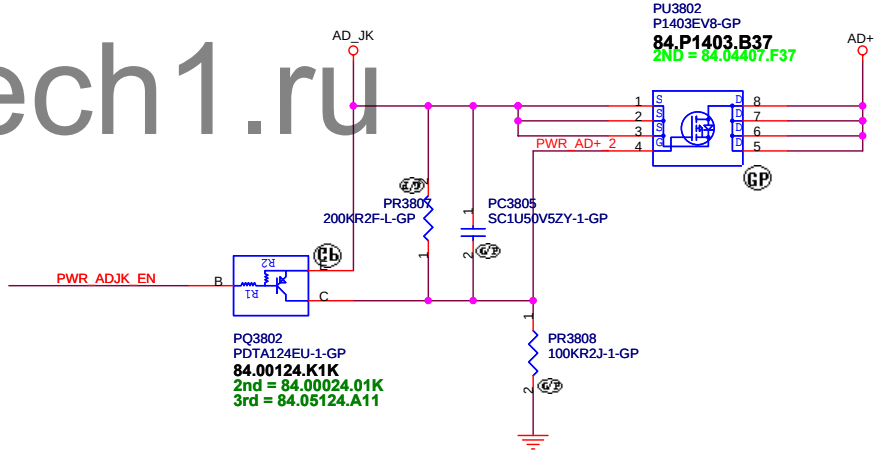

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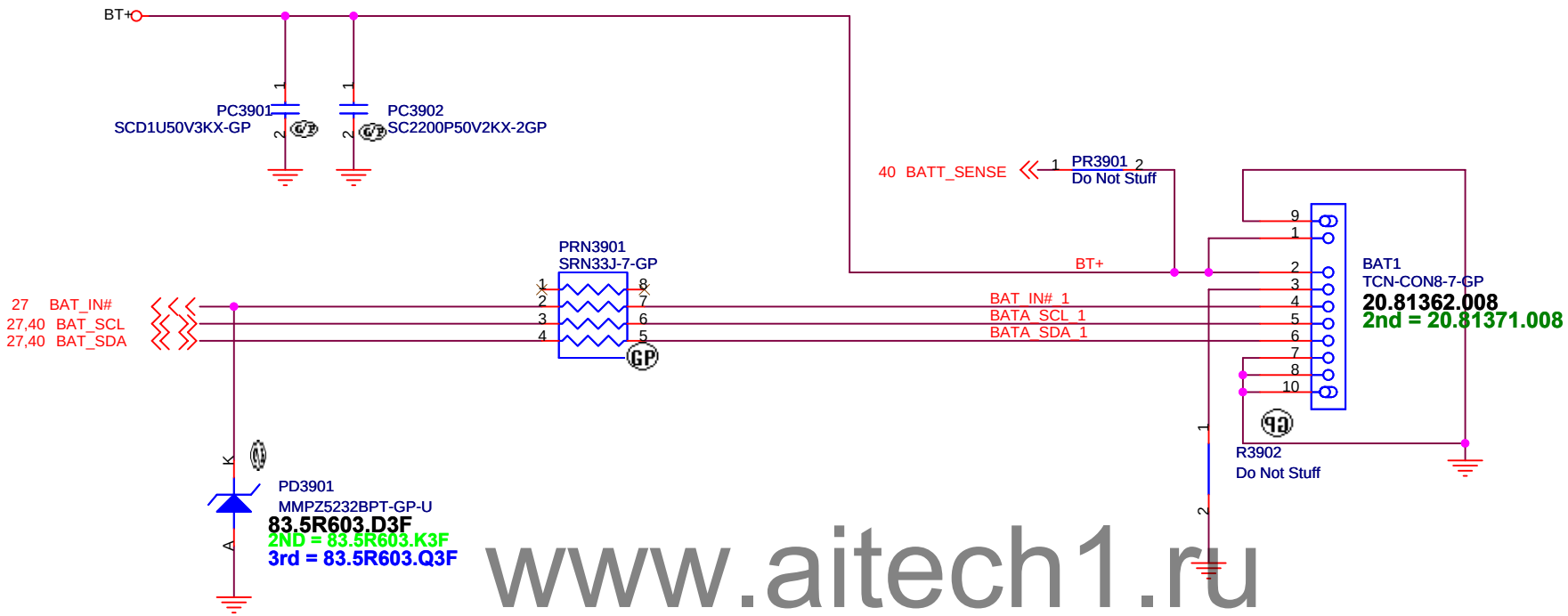

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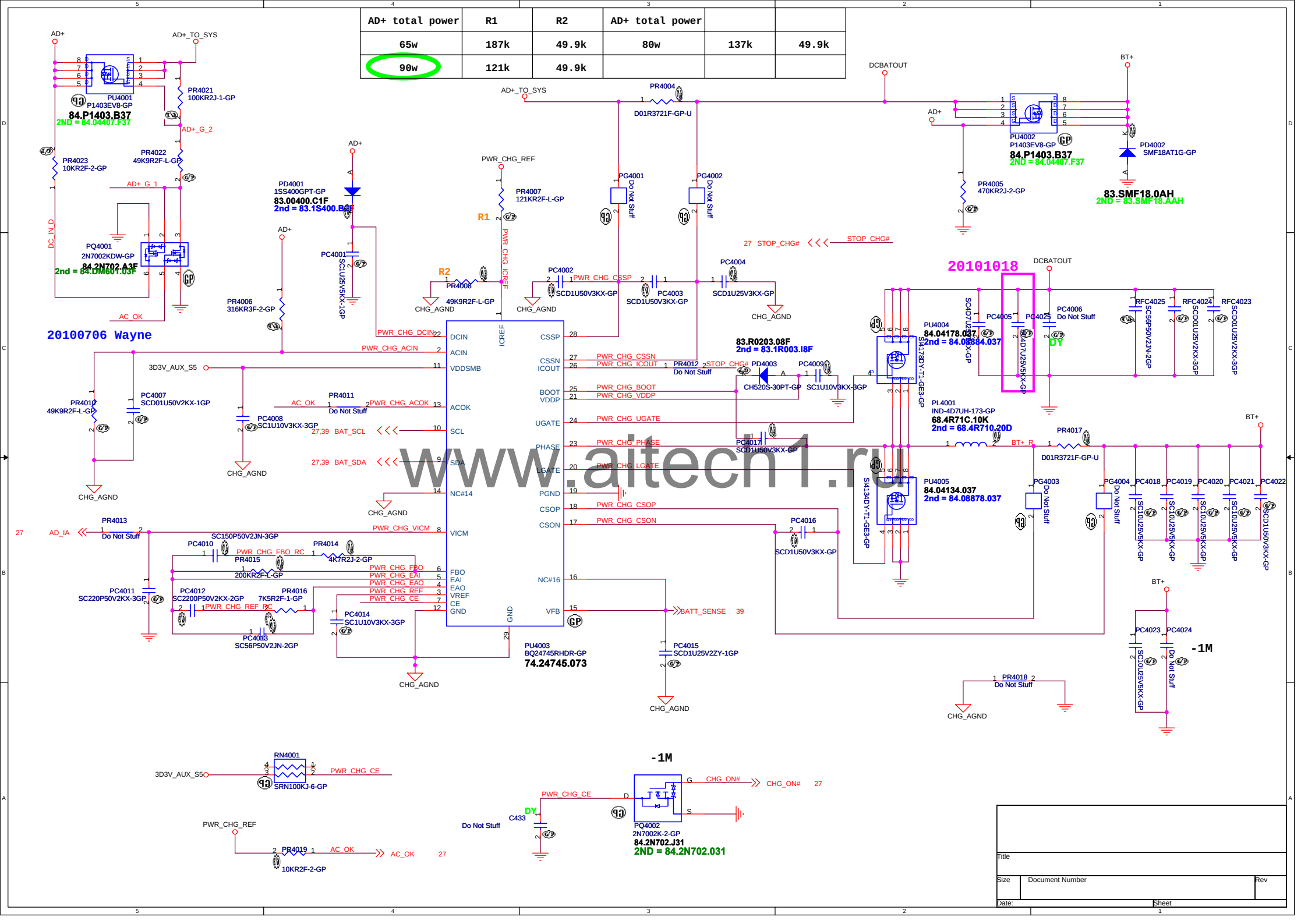
AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



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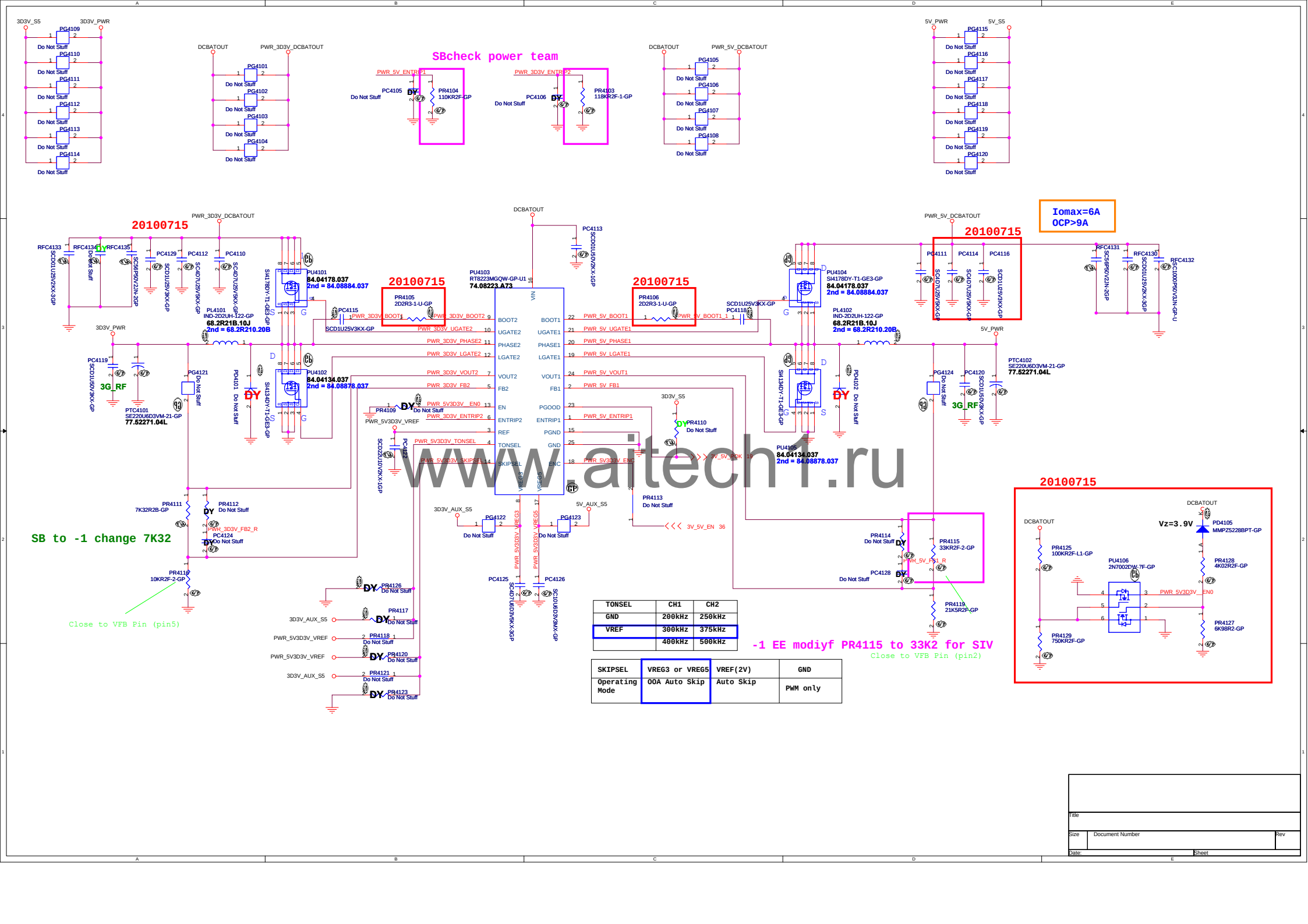
SBcheck power team
20100715
20100715
20100715
20100715
Iomax=6A
OCP>9A
SB to -1 change 7K32
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
-1 EE modiyf PR4115 to 33K2 for SIV
Vz=3.9V
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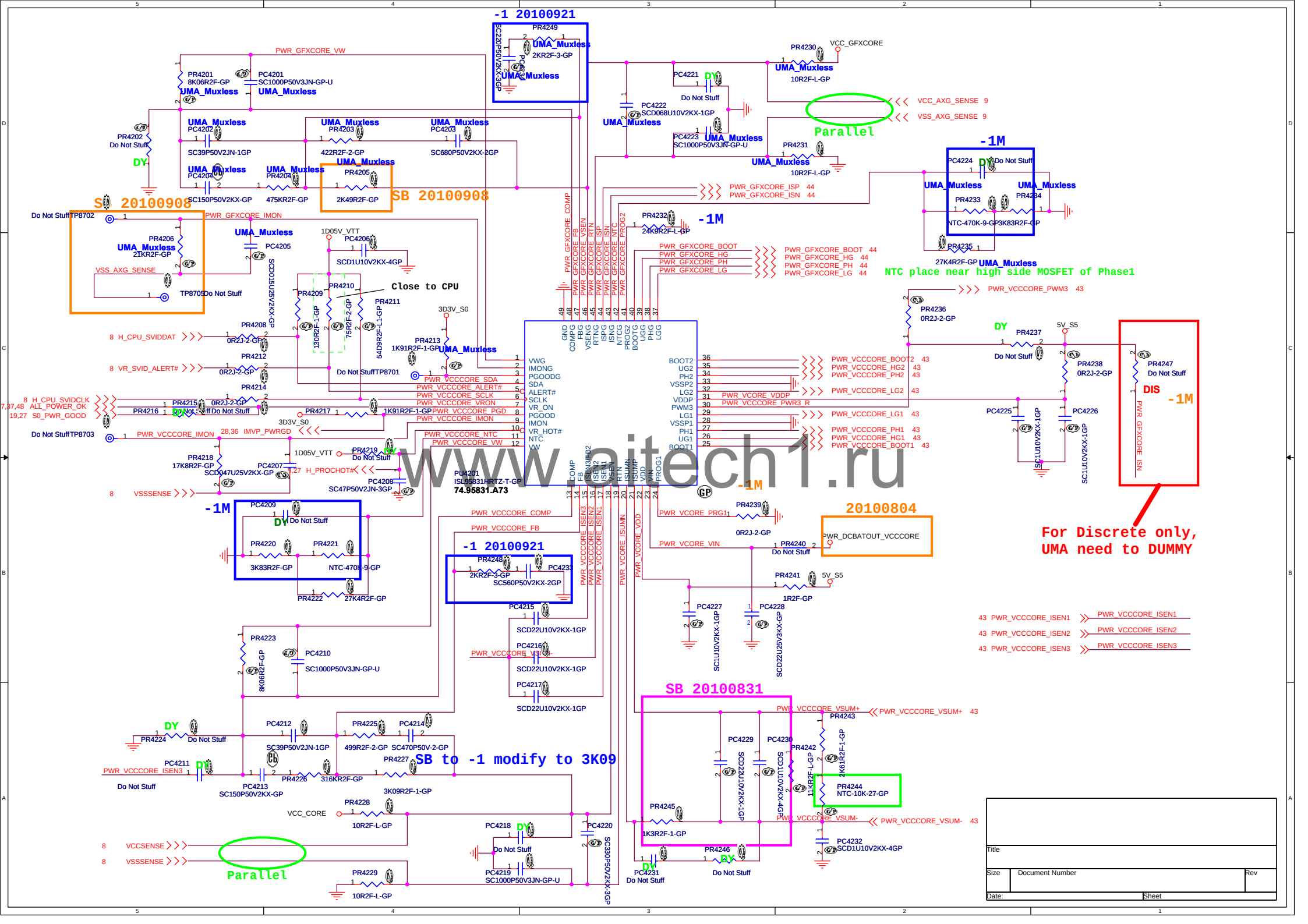
PU4103
RT8223MGQW-GP-U1
74.08223.A73
PU4101
84.04178.037
2nd = 84.08884.037
PU4102
84.04134.037
2nd = 84.08878.037
PU4104
SI4178DY-T1-GE3-GP
84.04178.037
2nd = 84.08884.037
PU4105
84.04134.037
2nd = 84.08878.037
PU4102
IND-2D2UH-122-GP
68.2R21B.10J
2nd = 68.2R210.20B
PU4106
2N7002DW-7F-GP
PD4105
MMPZ5228BPT-GP
PTC4101
SE220U6D3VM-21-GP
77.52271.04L
PTC4102
SE220U6D3VM-21-GP
77.52271.04L
PR4103 118KR2F-1-GP
PR4104 110KR2F-GP
PR4105 2D2R3-1-U-GP
PR4106 2D2R3-1-U-GP
PR4111 7K32R2B-GP
PR4112 Do Not Stuff
PR4113 Do Not Stuff
PR4114 Do Not Stuff
PR4115 33KR2F-2-GP
PR4116 10KR2F-2-GP
PR4119 21K5R2F-GP
PR4125 100KR2F-L1-GP
PR4127 6K98R2-GP
PR4128 4K02R2F-GP
PR4129 750KR2F-GP
PC4124 Do Not Stuff
PC4128 Do Not Stuff
PWR_3D3V_FB2_R
PWR_5V_FB1_R
PWR_5V3D3V_EN0
3V_5V_EN
3V_5V_OK
PWR_5V3D3V_VREF
PWR_5V3D3V_TONSEL
PWR_5V3D3V_SKIPSEL
PWR_5V3D3V_ENC
PWR_5V_ENTRIP1
PWR_3D3V_ENTRIP2
PWR_3D3V_BOOT2
PWR_3D3V_UGATE2
PWR_3D3V_PHASE2
PWR_3D3V_LGATE2
PWR_3D3V_VOUT2
PWR_3D3V_FB2
PWR_5V_BOOT1
PWR_5V_UGATE1
PWR_5V_PHASE1
PWR_5V_LGATE1
PWR_5V_VOUT1
PWR_5V_FB1
3G_RF
Do Not Stuff
DY
TONSEL | CH1 | CH2
GND | 200kHz | 250kHz
VREF | 300kHz | 375kHz
400kHz | 500kHz
SKIPSEL | VREG3 or VREG5 | VREF(2V) | GND
Operating Mode | OOA Auto Skip | Auto Skip | PWM only


-1 20100921
SB 20100908
-1M
NTC place near high side MOSFET of Phase1
Close to CPU
Parallel
20100804
PWR_DCBATOUT_VCCCORE
For Discrete only,
UMA need to DUMMY
SB 20100831
SB to -1 modify to 3K09
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
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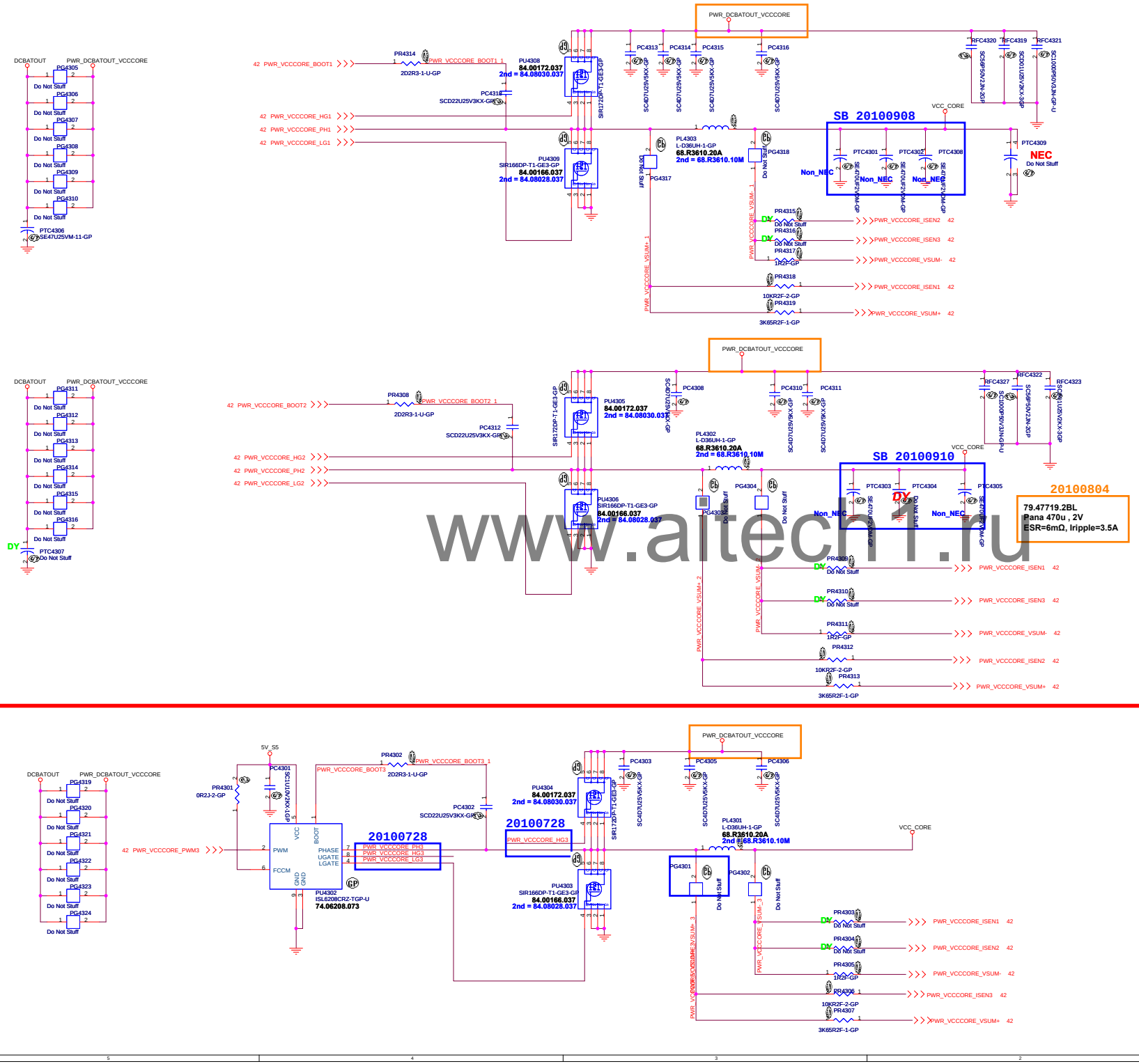

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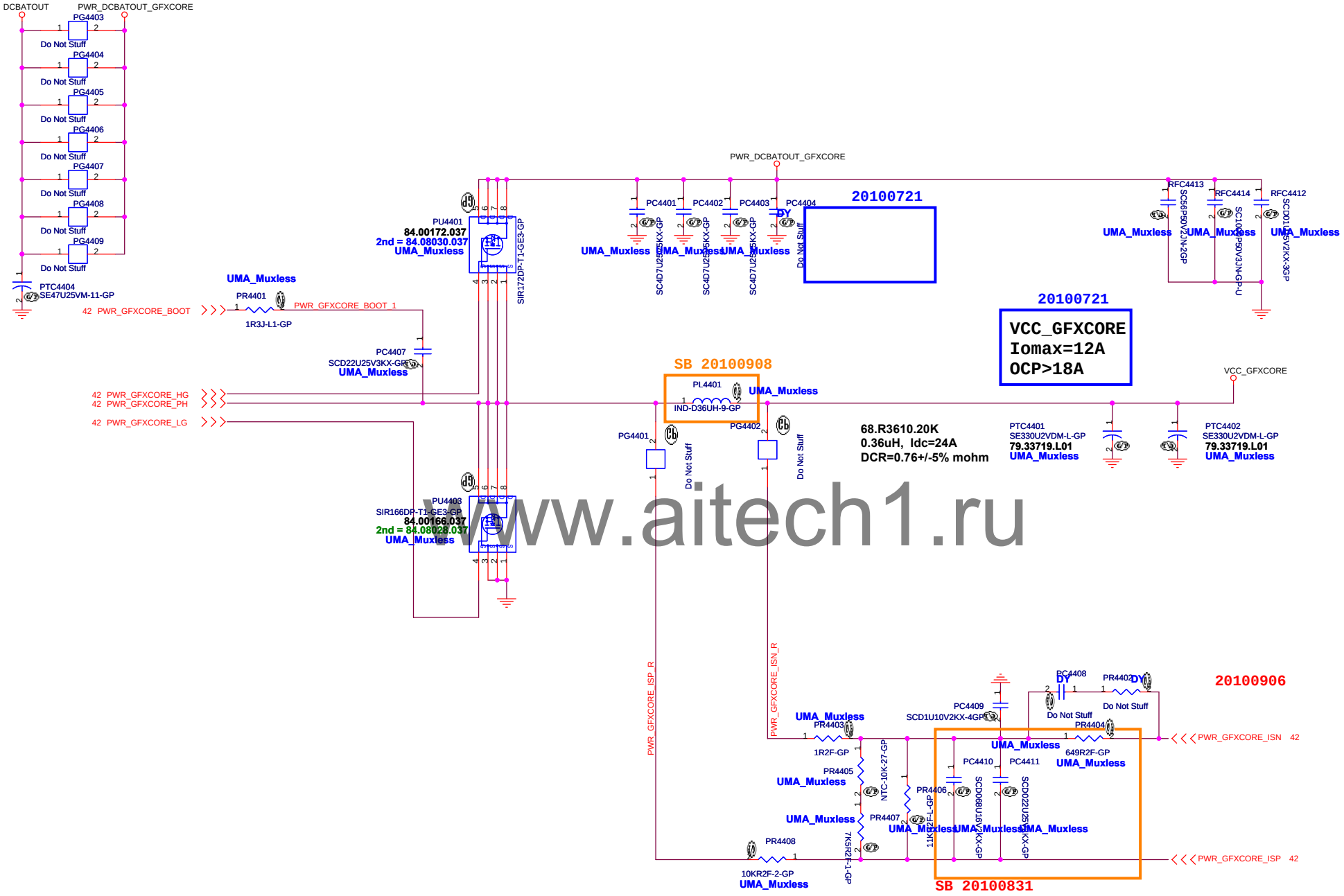

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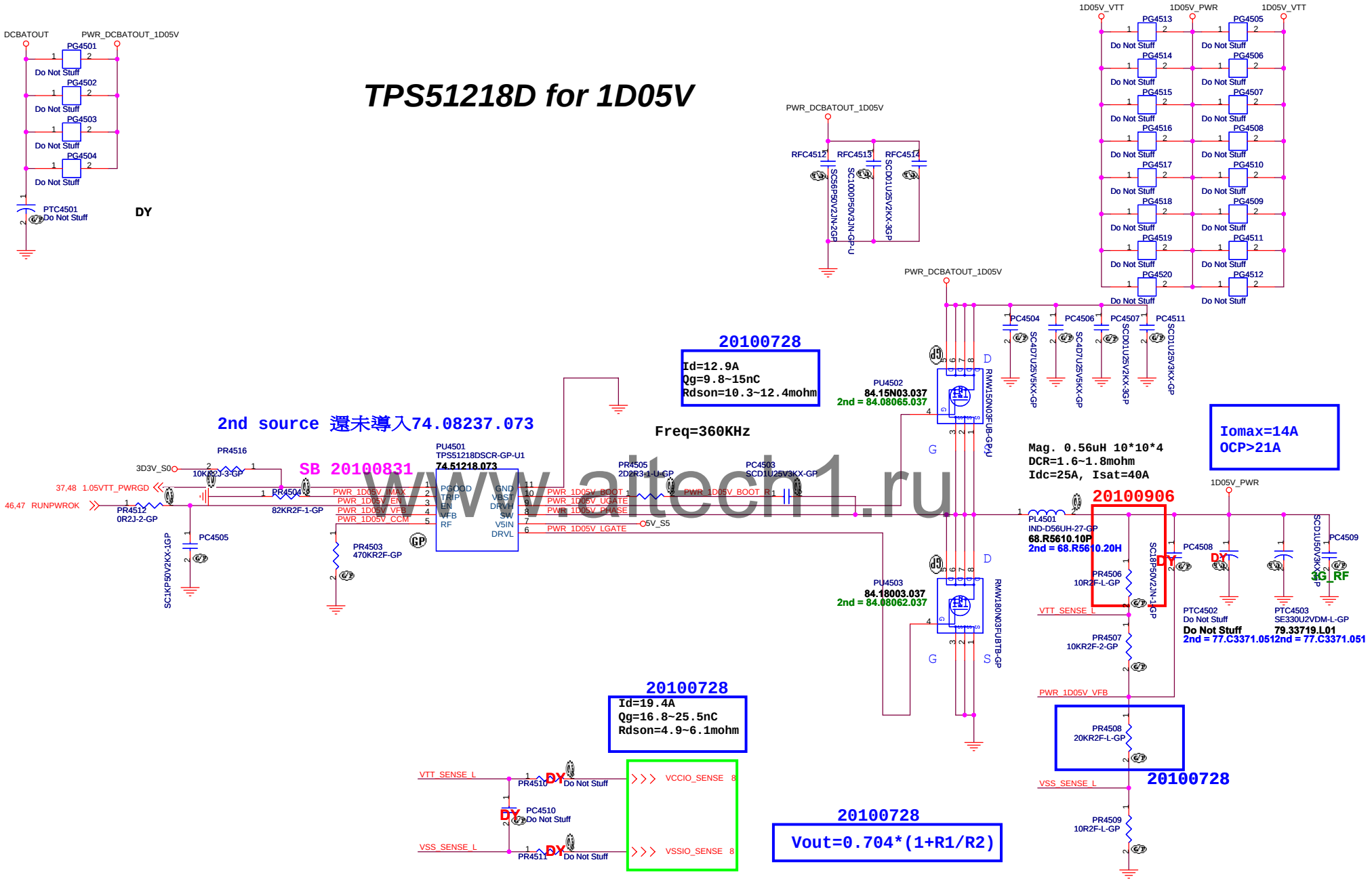
TPS51218D for 1D05V



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SSID = PWR.Plane.Regulator_1p5v0p75v

RT8207L for 1D5V

20100805

SB 20100831

20100728

Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

20100906

SB

Mag. 1.0uH 10*10*4
DCR=2.9~3.3mohm
Idc=18A, Isat=36A

Iomax=12A
OCP>20A

Close to pin23

Close to pin23

20100728

Close to output cap pin1, not inside of the output cap

2nd source 還未導入74.51116.073

Close to PIN9

20100728

Vout=0.75*(1+R1/R2)

SB R4608 chekc 修改31K6R
Vout 需再1.55V 以上

+0.75VS
Iomax: 1.2A

DY

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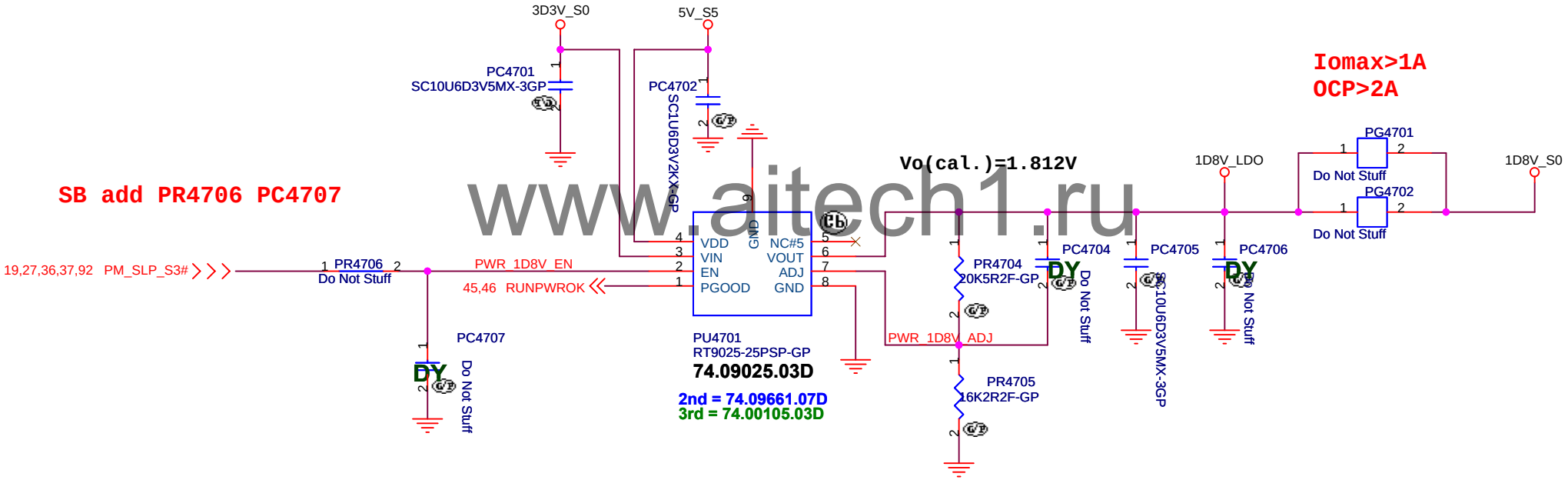
SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



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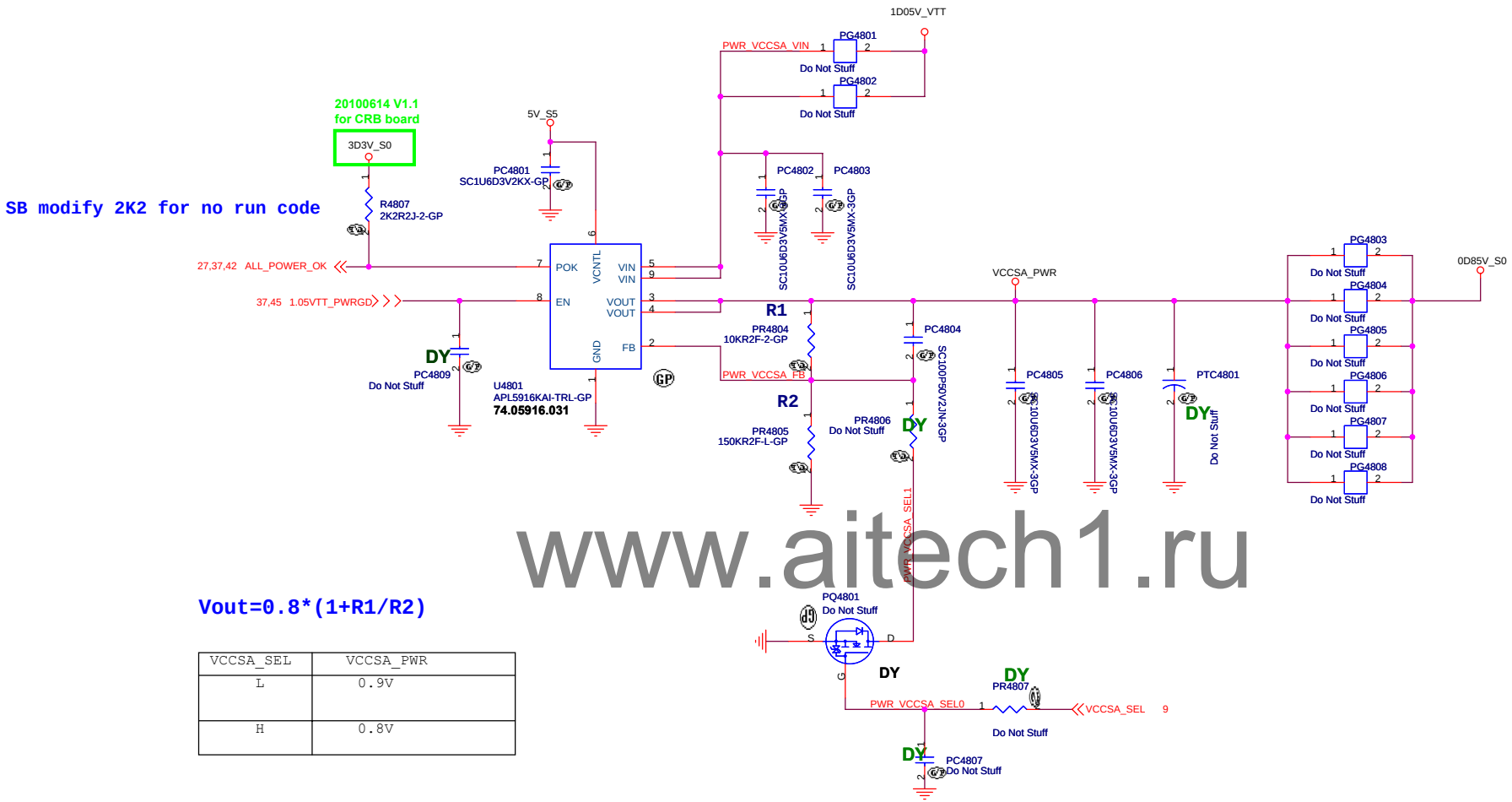
APL5916 for VCCSA



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Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

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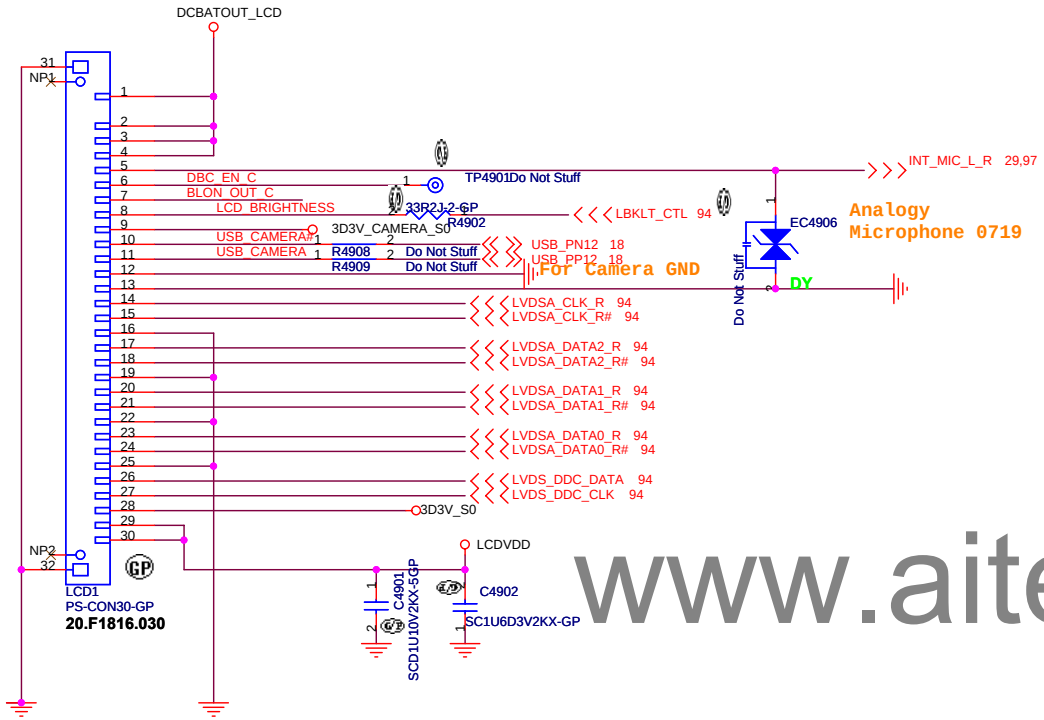
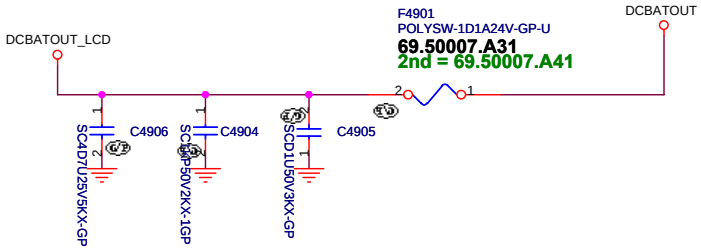
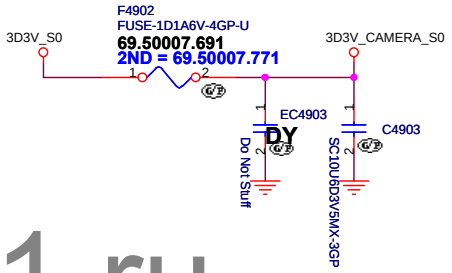
LVDS CONNECTOR



INVERTER POWER



Camera Power



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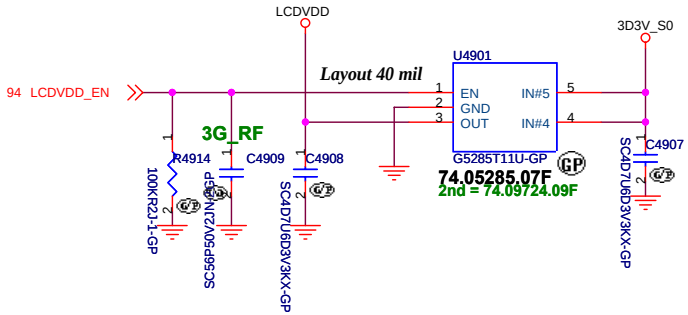
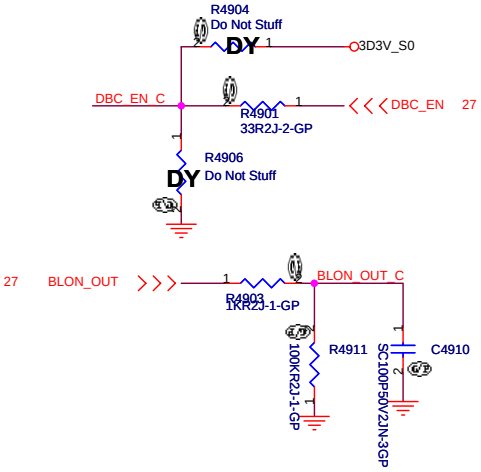
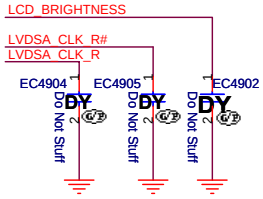
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



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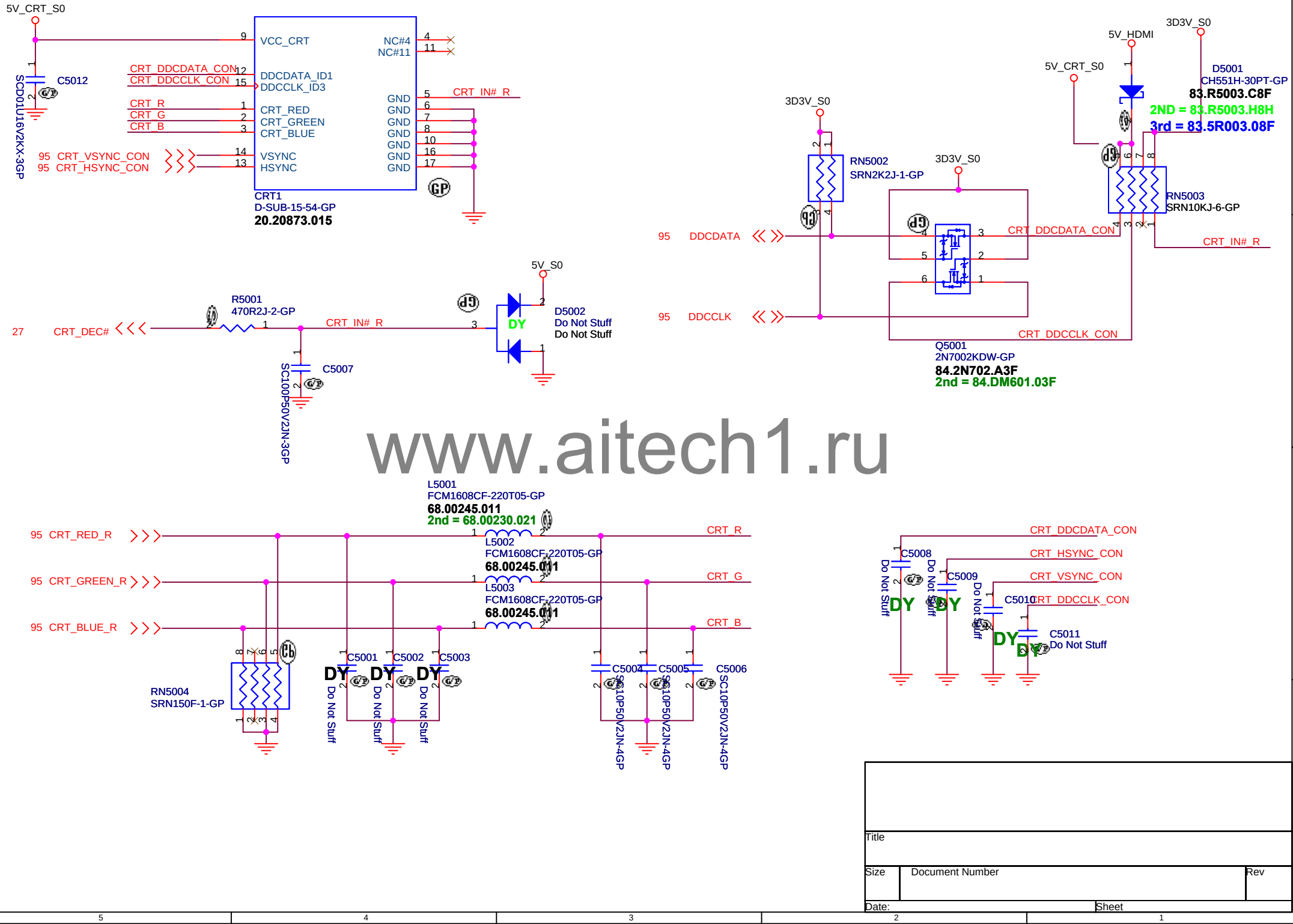

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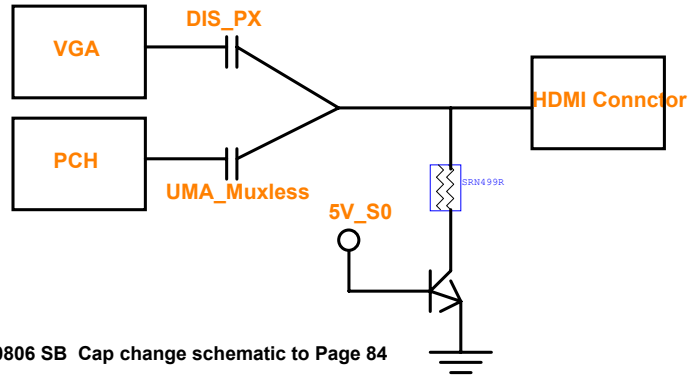
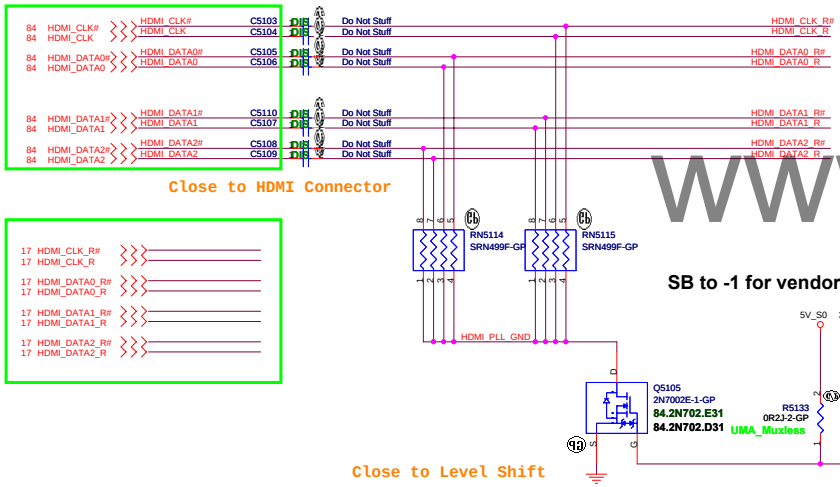
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

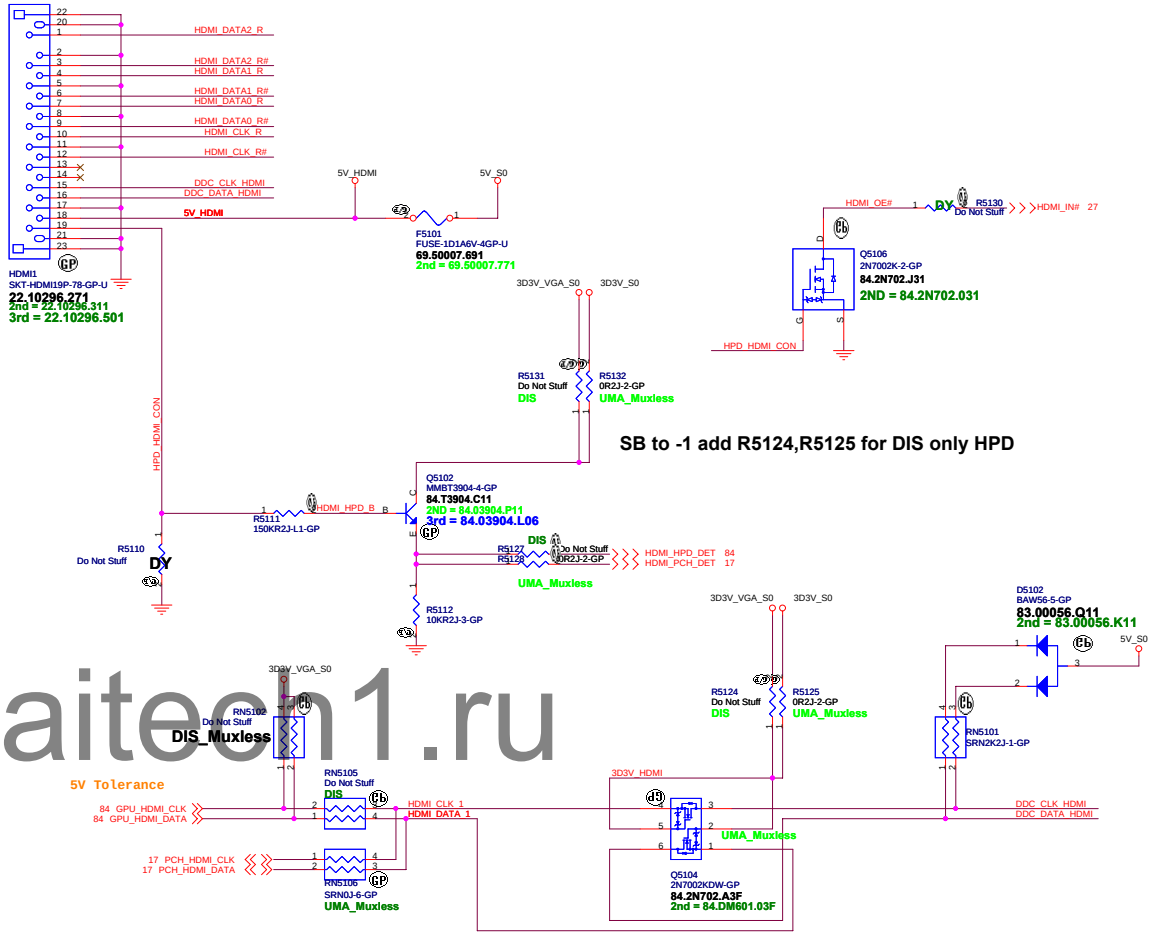
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



HDMI CONN



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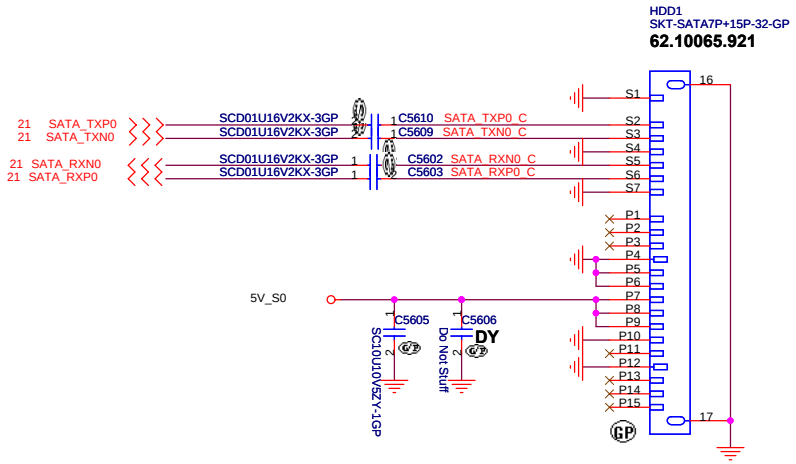
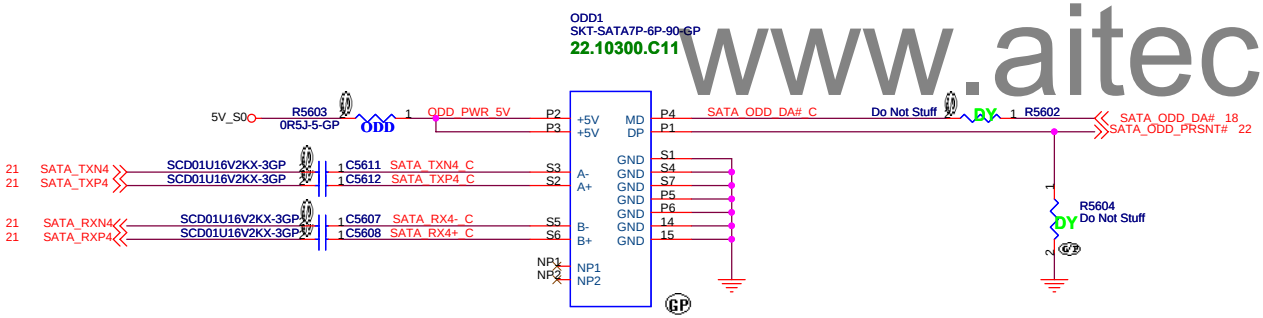
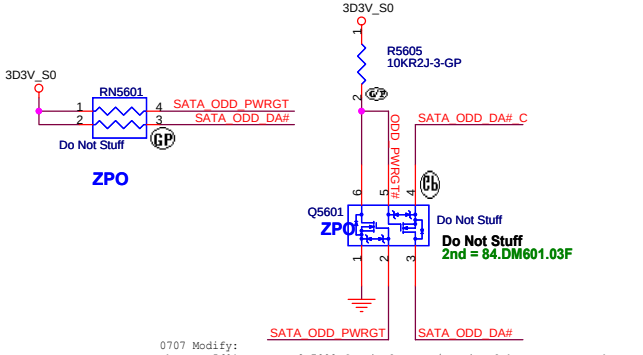


ODD Connector



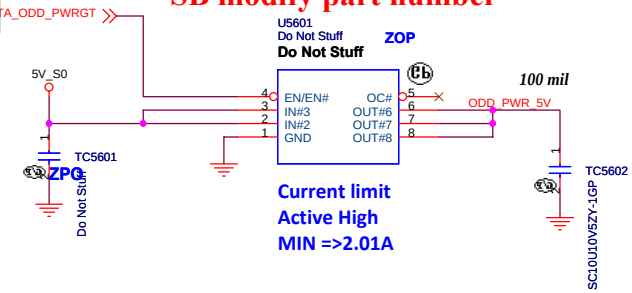


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



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GIGA Lan Transformer

LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

SB modiyf Pin9 Pin10 SWAP

LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE

RJ45
RJ45-12P-16-GP
22.10321.Y21
2nd = 22.10321.Y91

RN5901
SRN470J-4-GP-U

EC5901 EC5902 Do Not Stuff DY

SB modify For EMI

U5901 U5902 U5903 U5904
TVLST2304AD0-GP
SURGE

GDT1 GDT2 GDT3 GDT4
SURGE

C5916 C5917 C5918 C5919 DY Do Not Stuff

EC5907 EC5908 EC5909 EC5910 Do Not Stuff

C5905 SC1KP2KV6KX-GP

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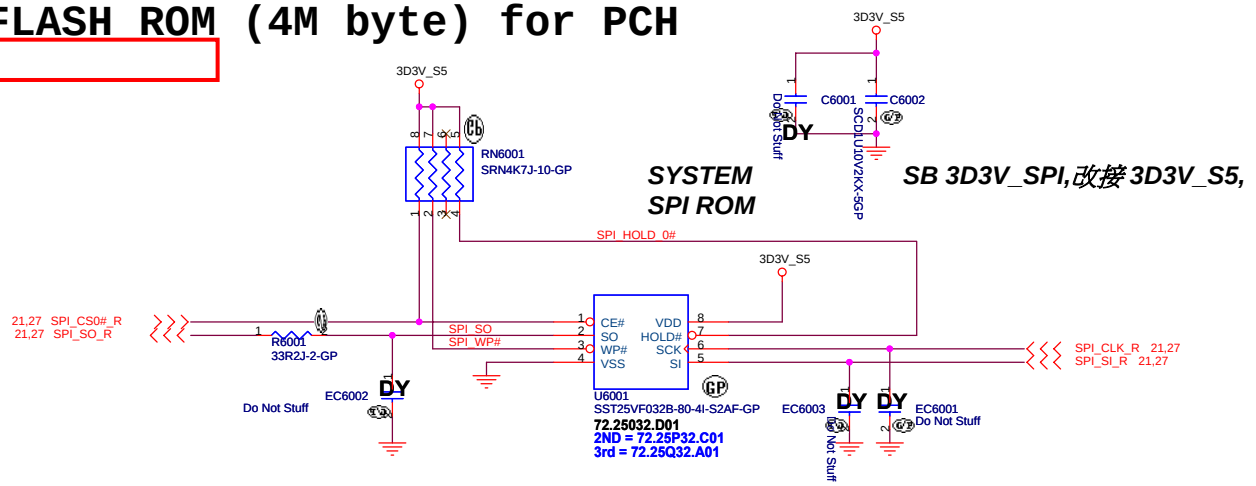
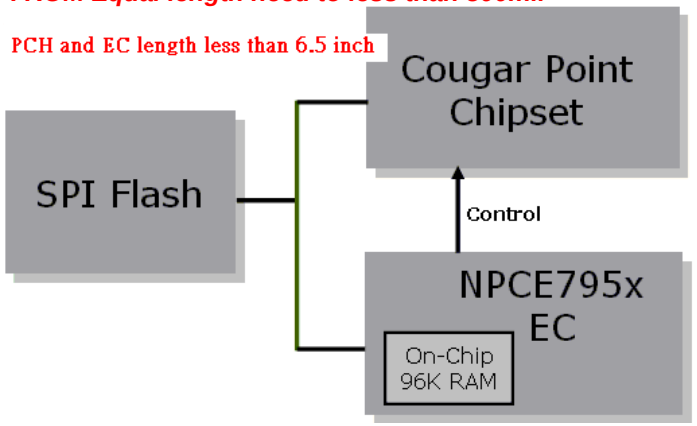
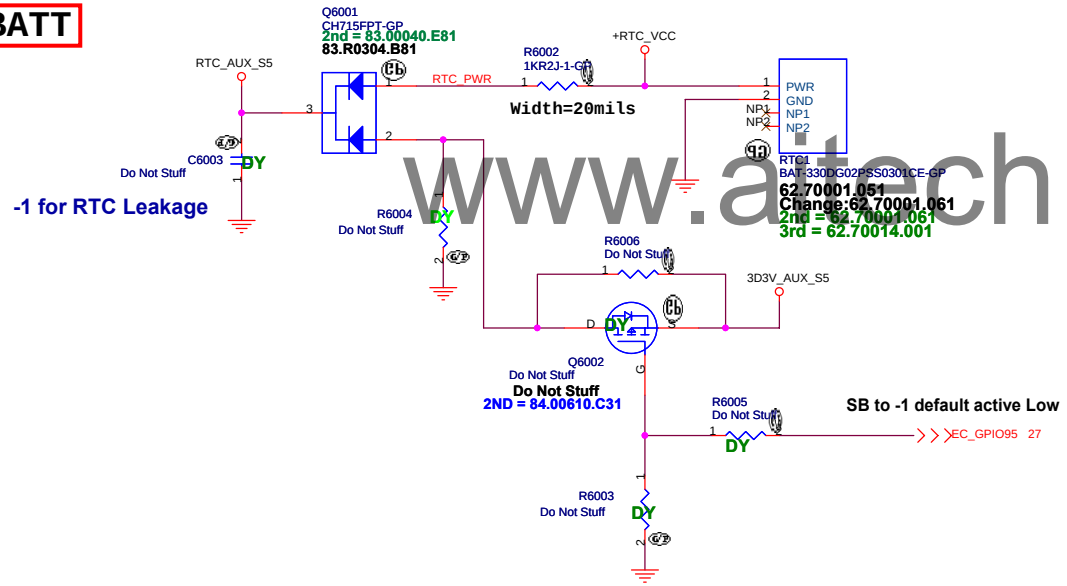
SPI FLASH ROM (4M byte) for PCH





SSID = RBATT



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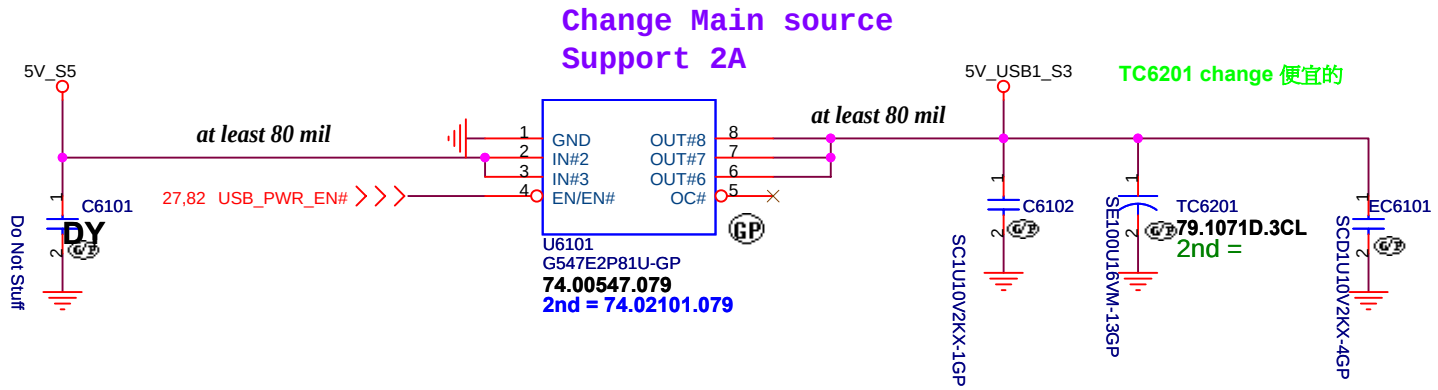

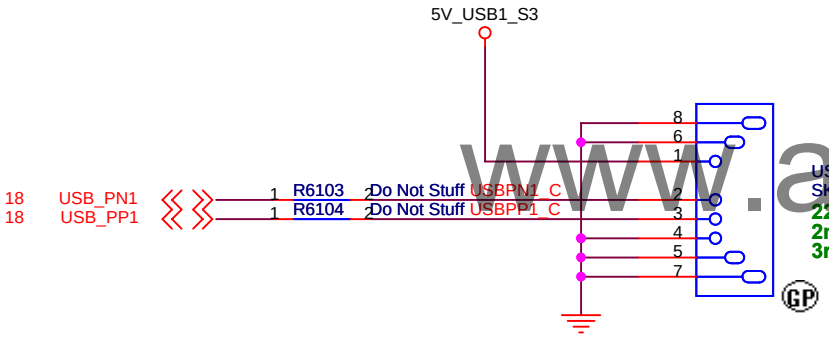

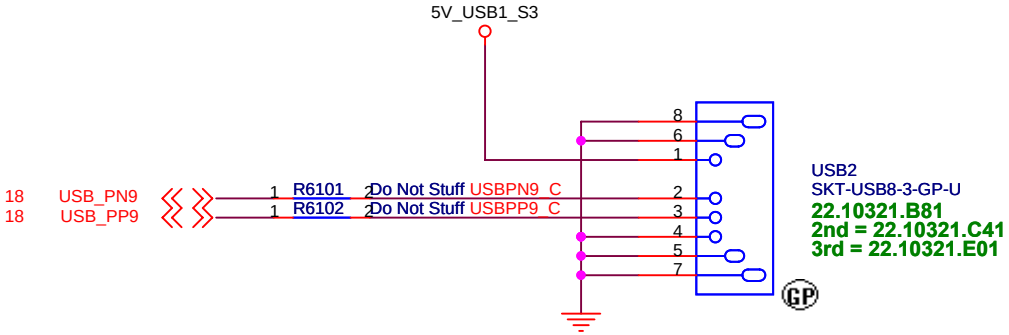

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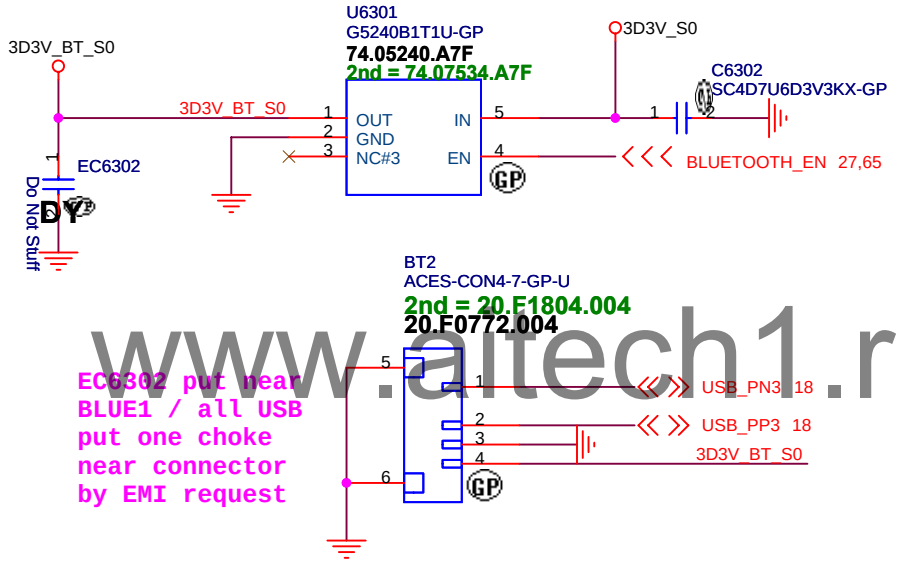
Bluetooth Module conn.

ANNIE Bluetooth Module



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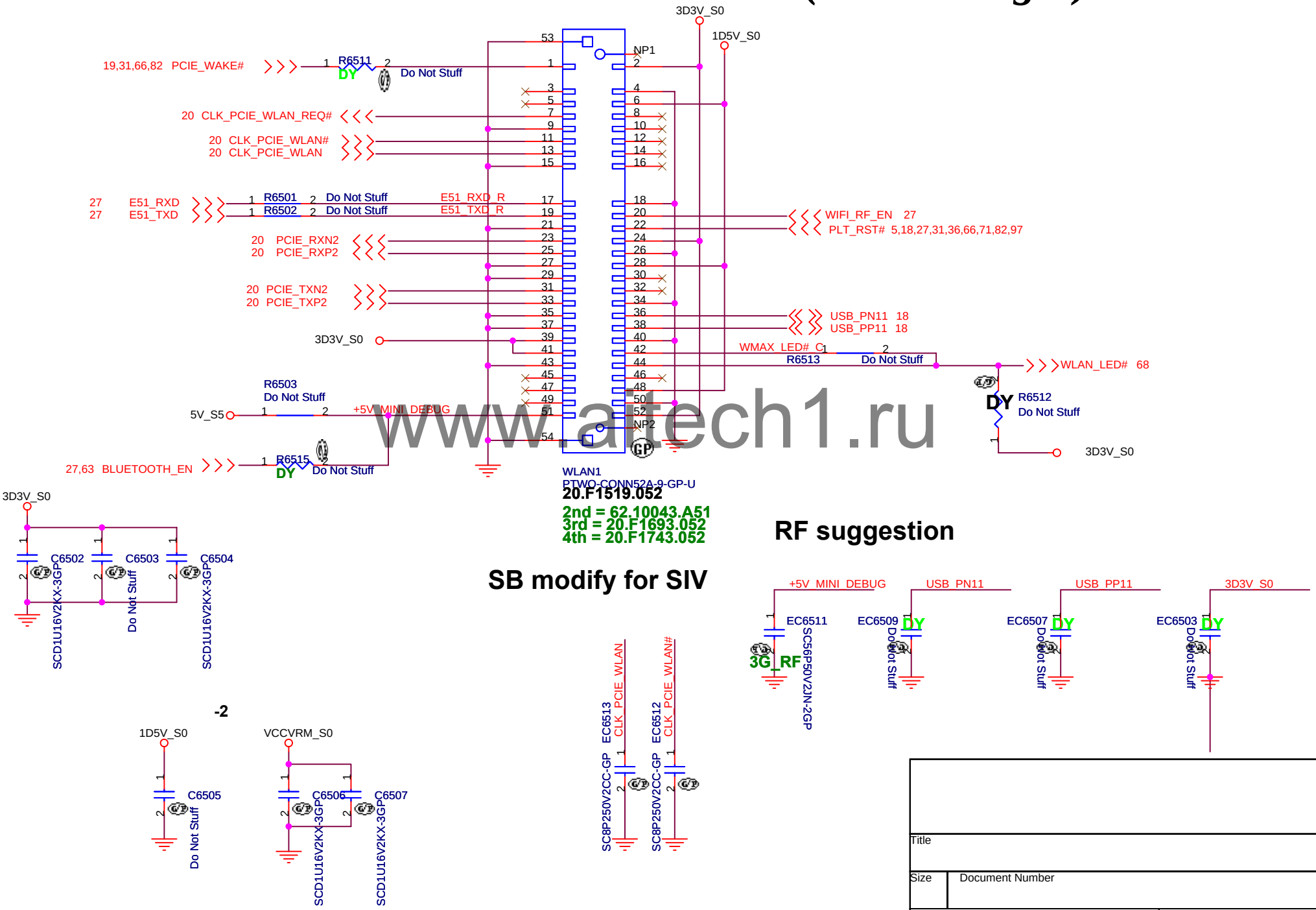
Mini Card Connector(802.11a/b/g/n)



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SB modify for SIV

RF suggestion

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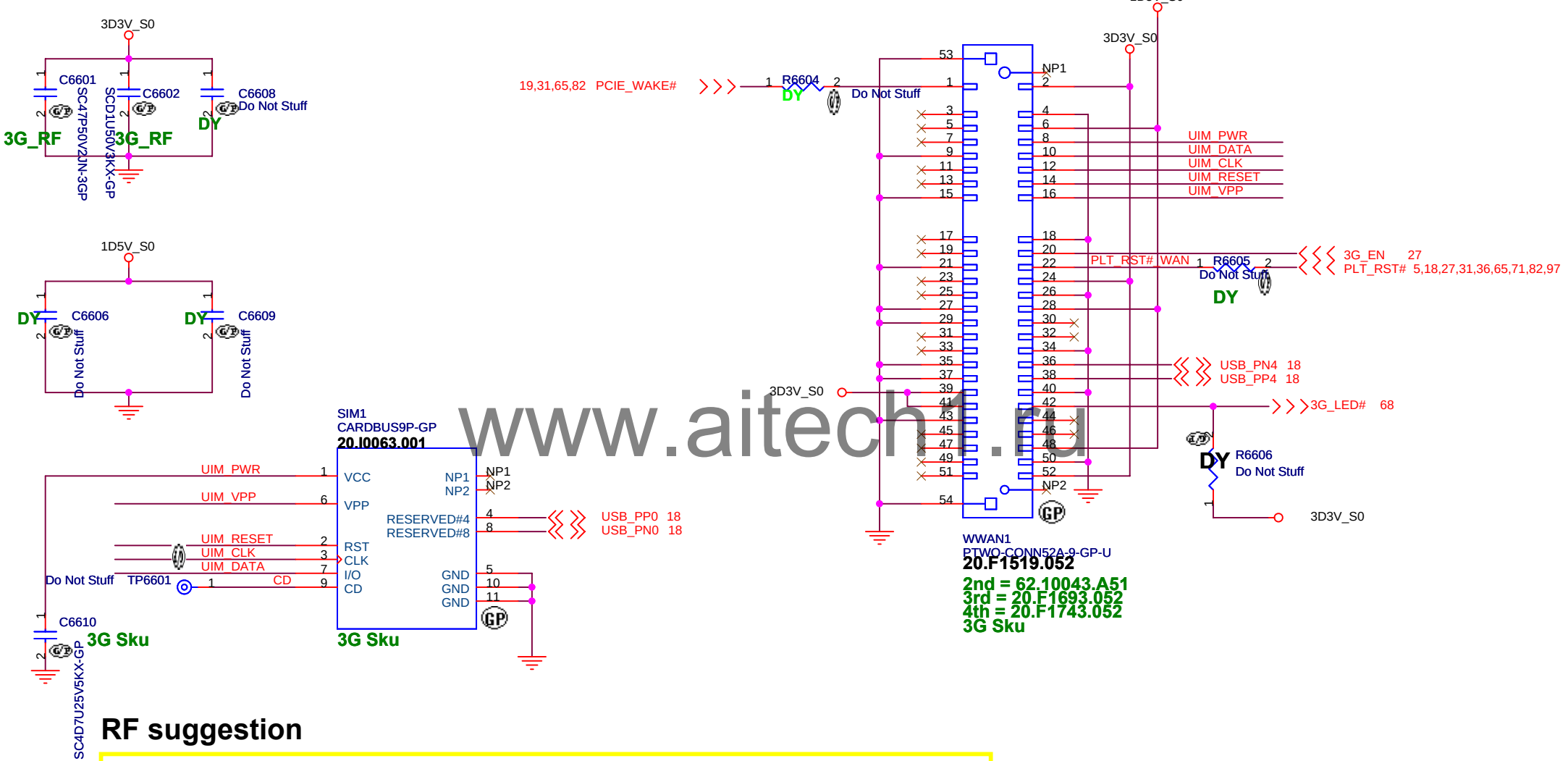
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



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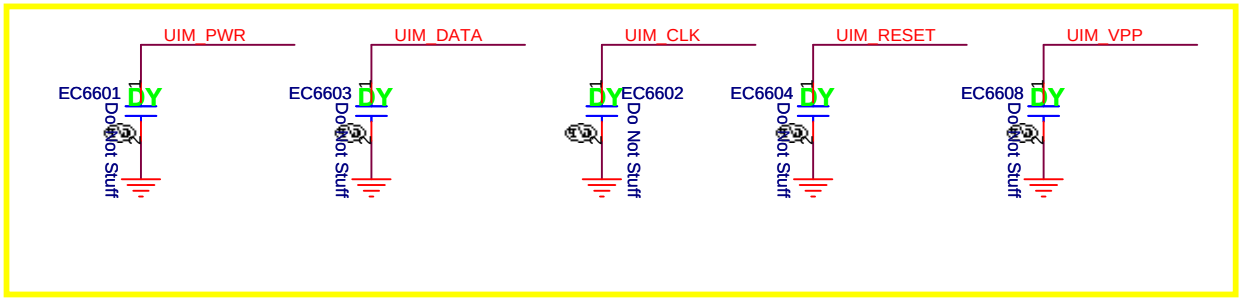
RF suggestion



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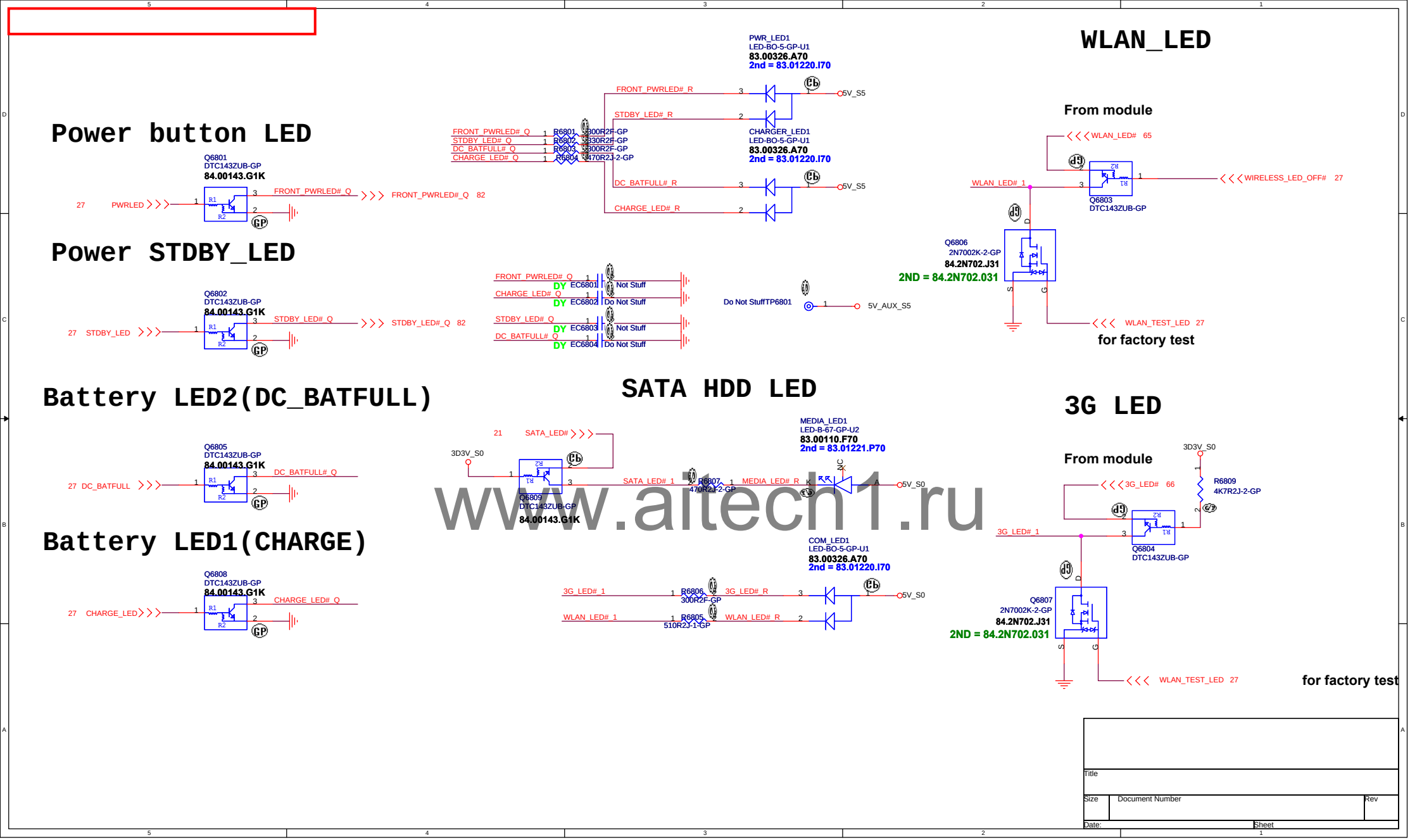

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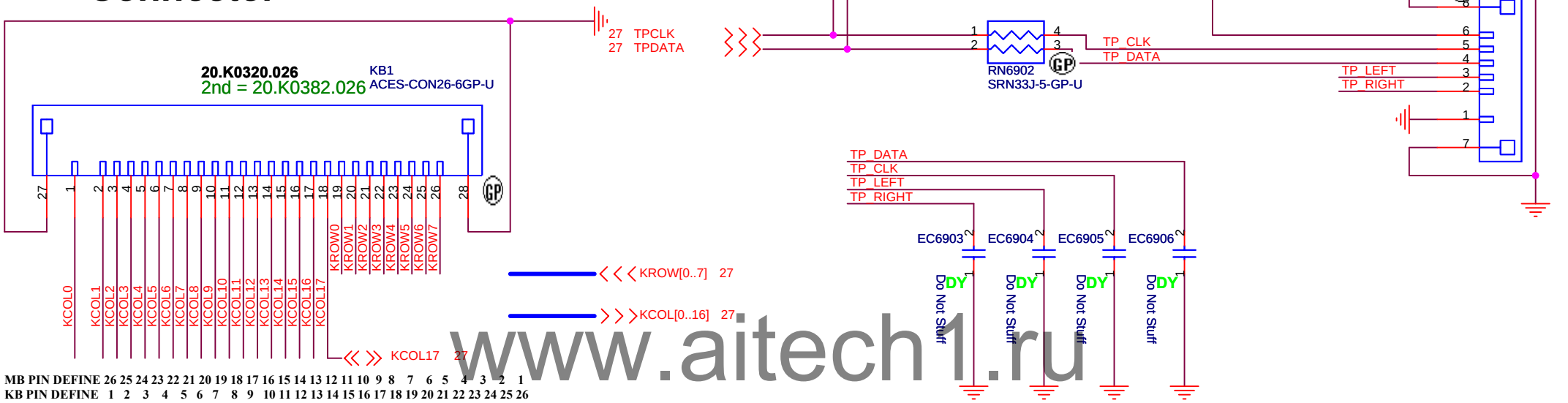
TOUCH PAD

FFC 異面

Internal KeyBoard Connector



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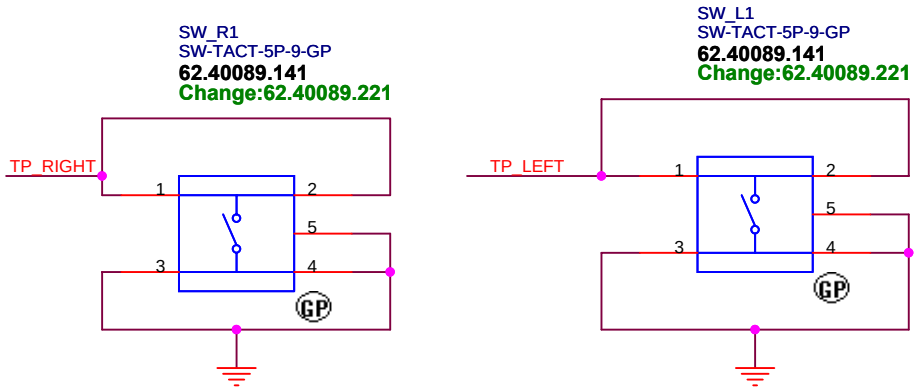
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1 **SB to -1 modify Part number**



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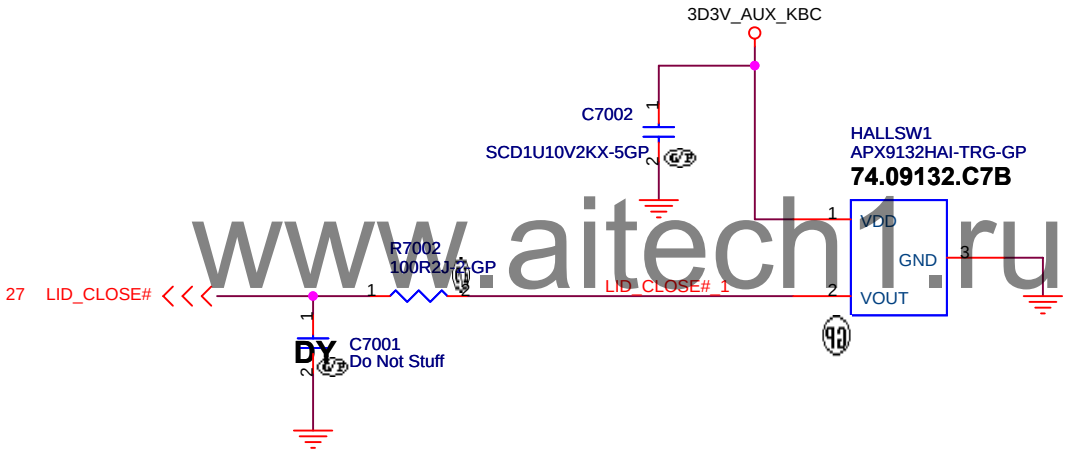

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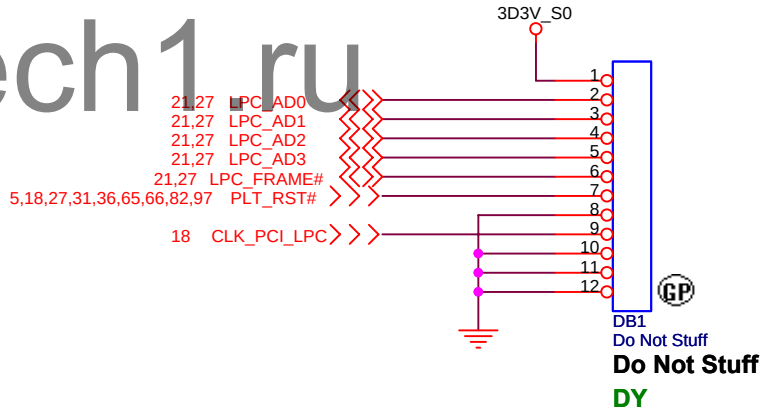

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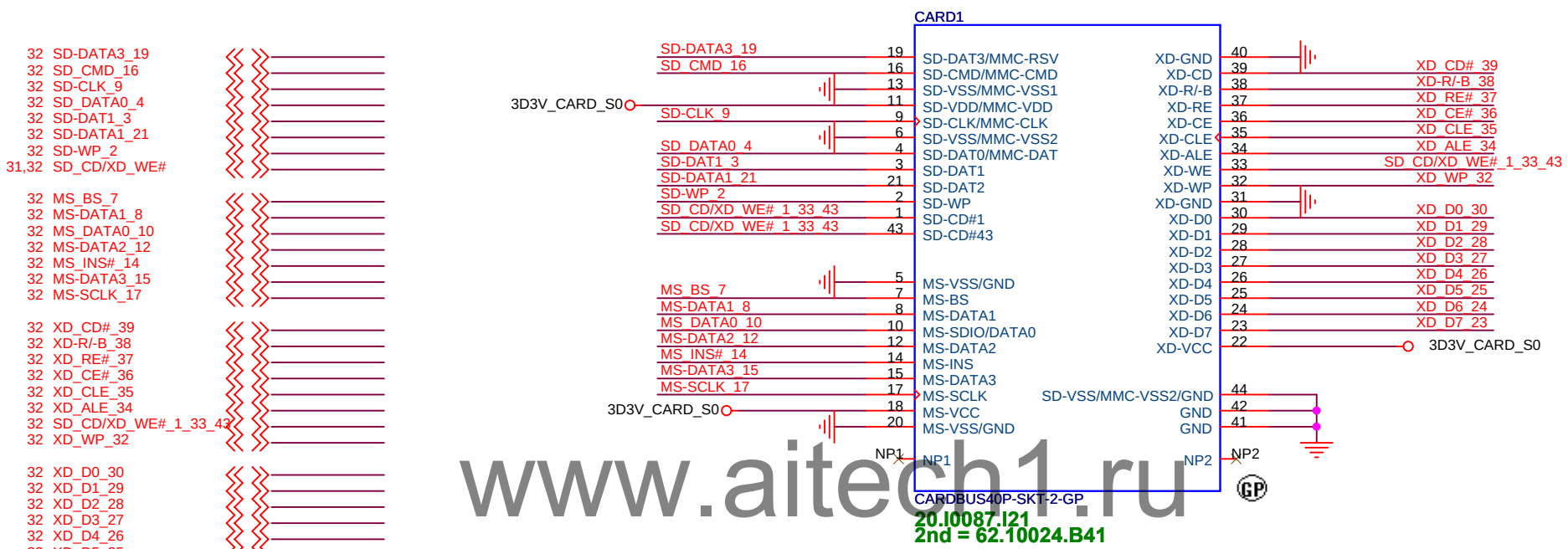
SD/XD/MS Card Reader



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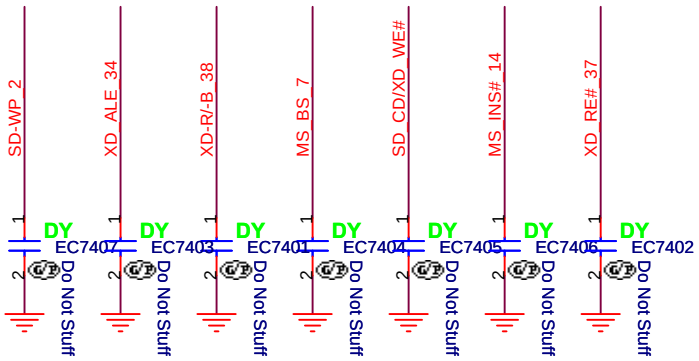

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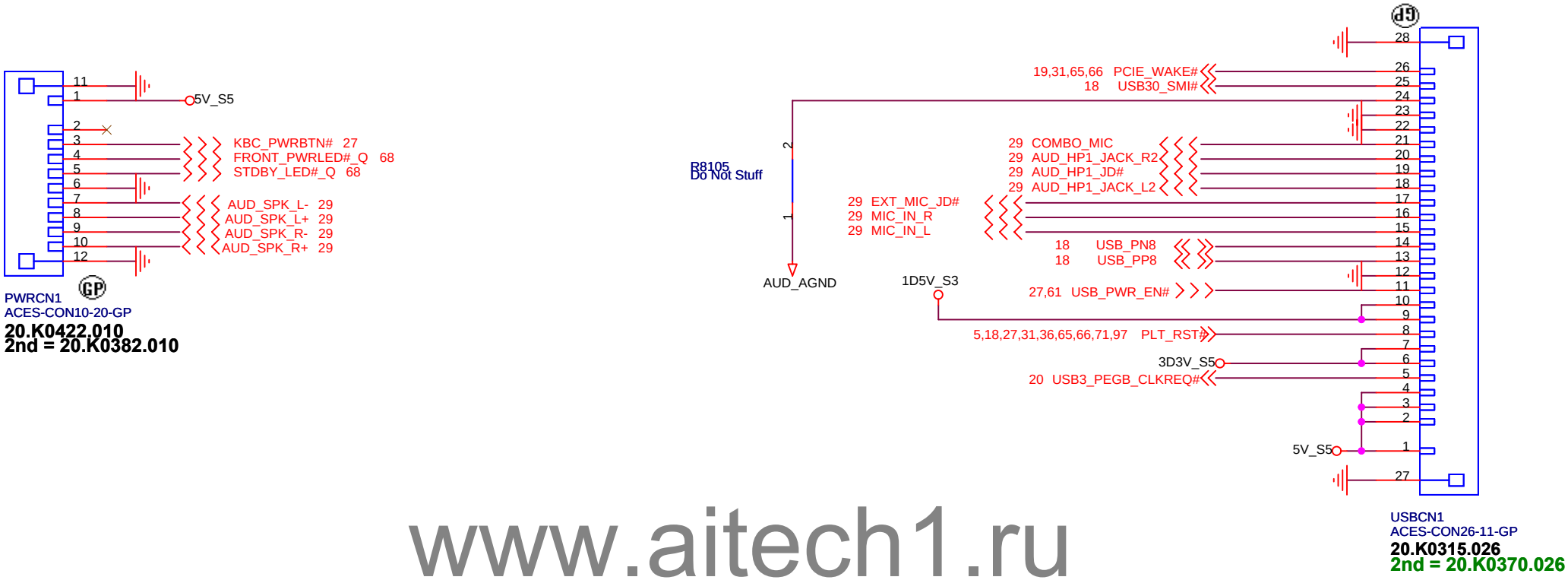

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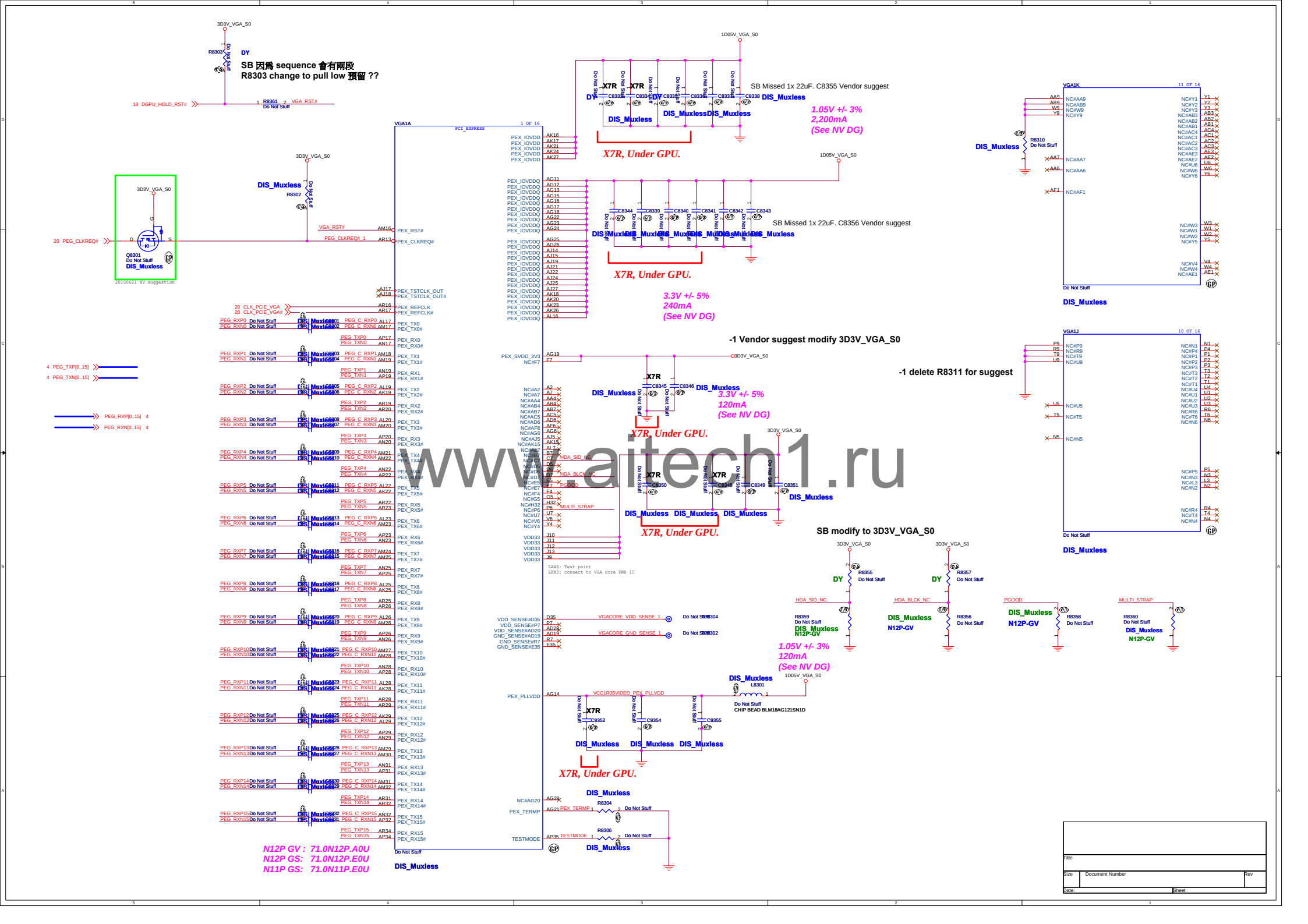
SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??
SB Missed 1x 22uF. C8355 Vendor suggest
1.05V +/- 3%
2,200mA
(See NV DG)
X7R, Under GPU.
SB Missed 1x 22uF. C8356 Vendor suggest
3.3V +/- 5%
240mA
(See NV DG)
-1 Vendor suggest modify 3D3V_VGA_S0
3.3V +/- 5%
120mA
(See NV DG)
-1 delete R8311 for suggest
SB modify to 3D3V_VGA_S0
1.05V +/- 3%
120mA
(See NV DG)
N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U
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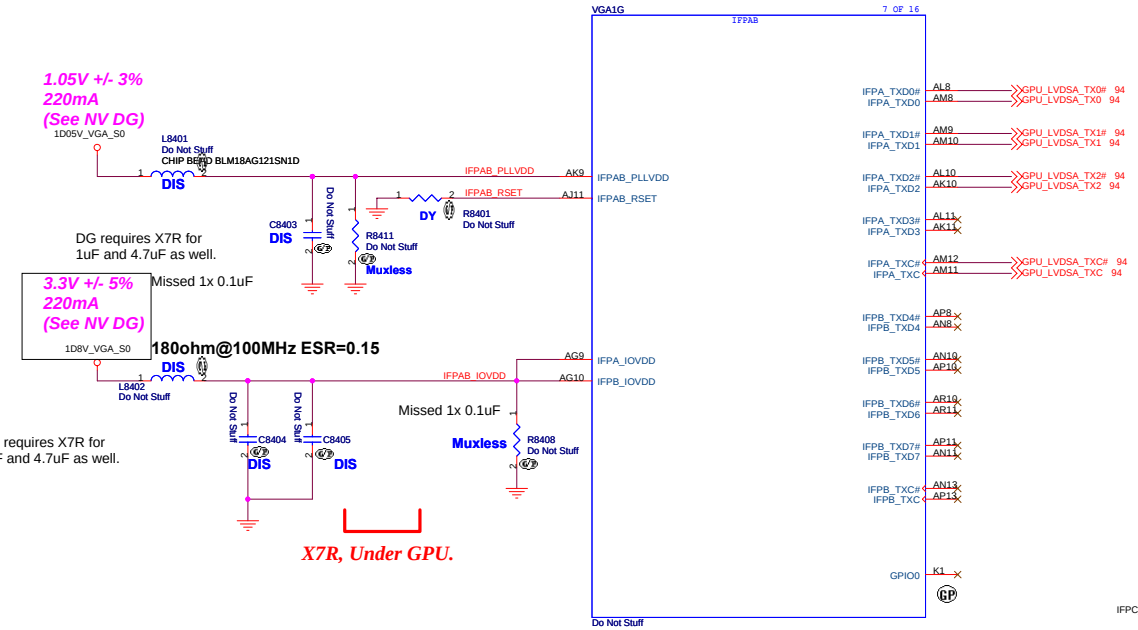
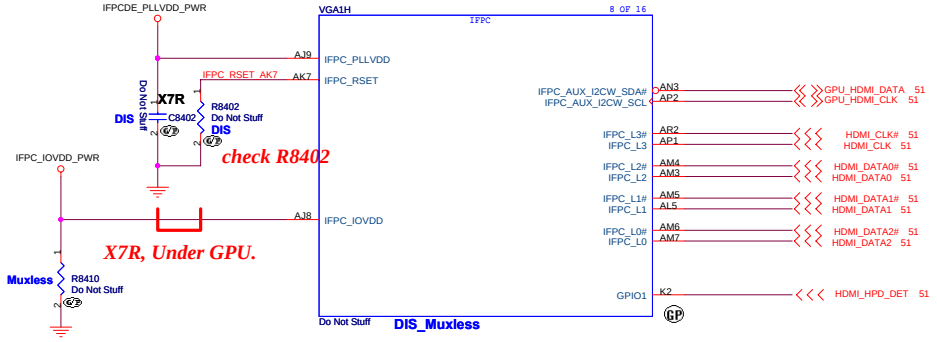
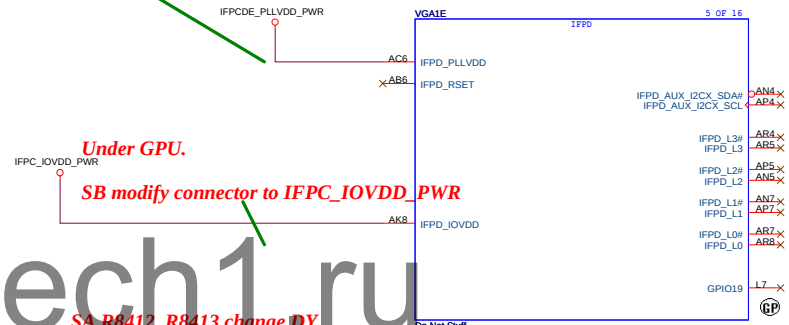
LVDS Interface

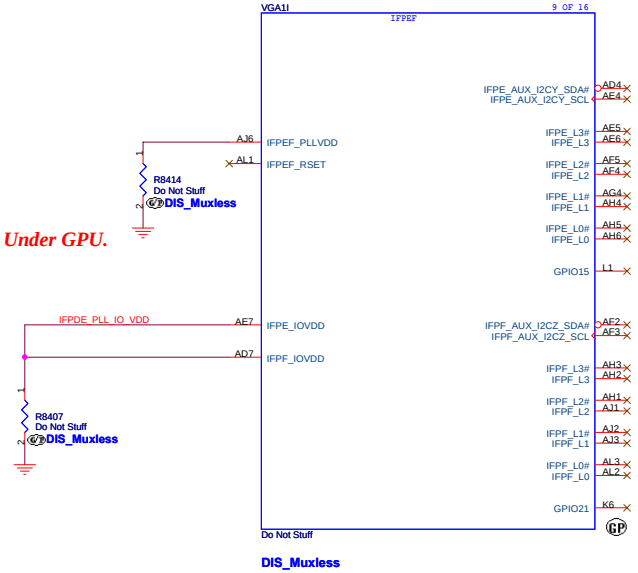




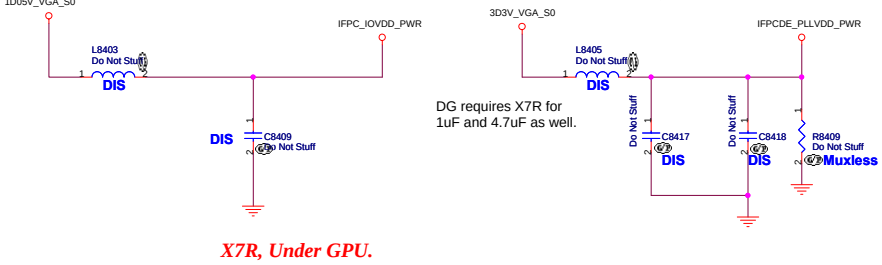
SB modify connector to IFPCDE_PLLVDD_PWR



SA R8412, R8413 change DY
SB R8412, R8413 change delete



HDMI Interface



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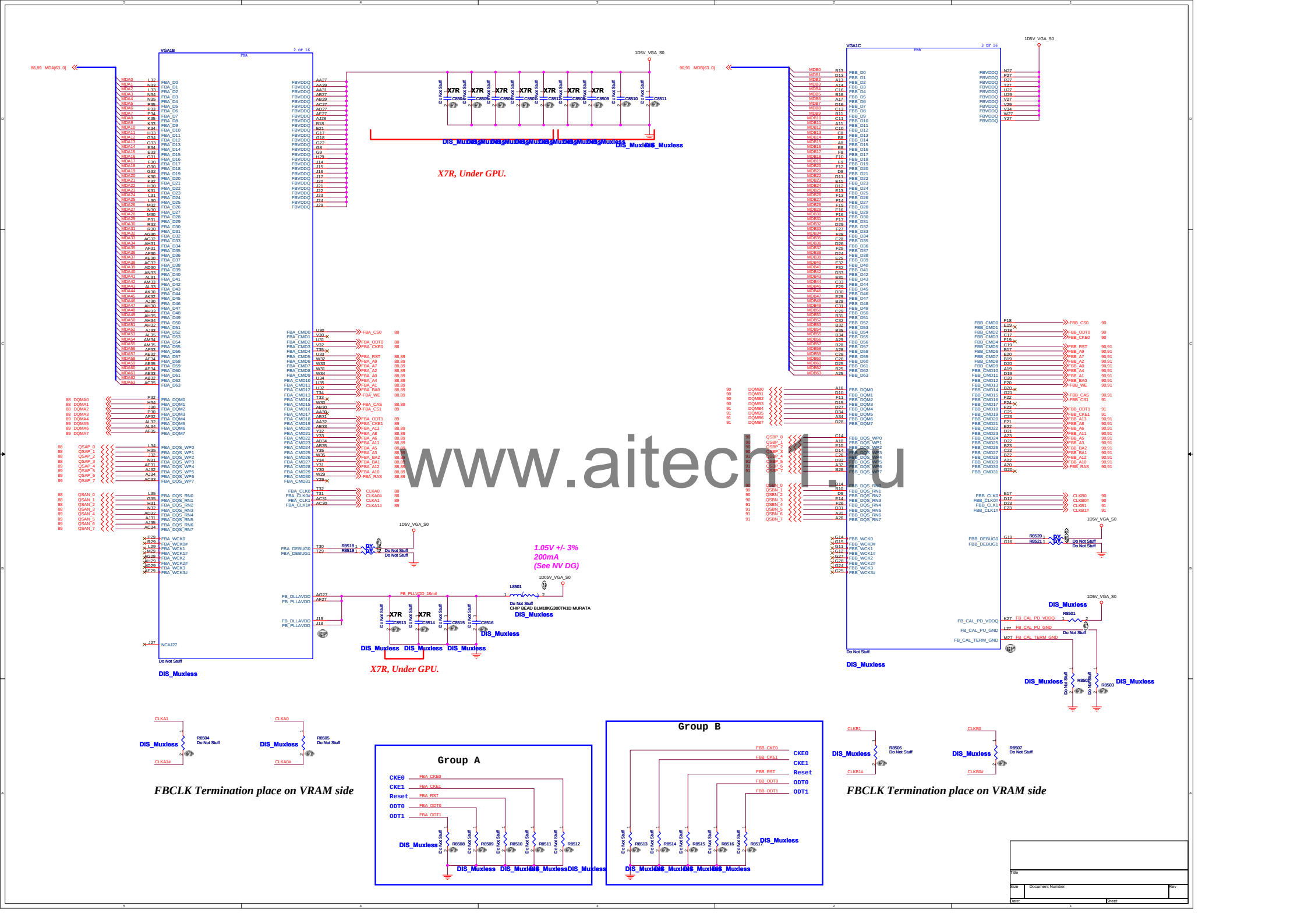

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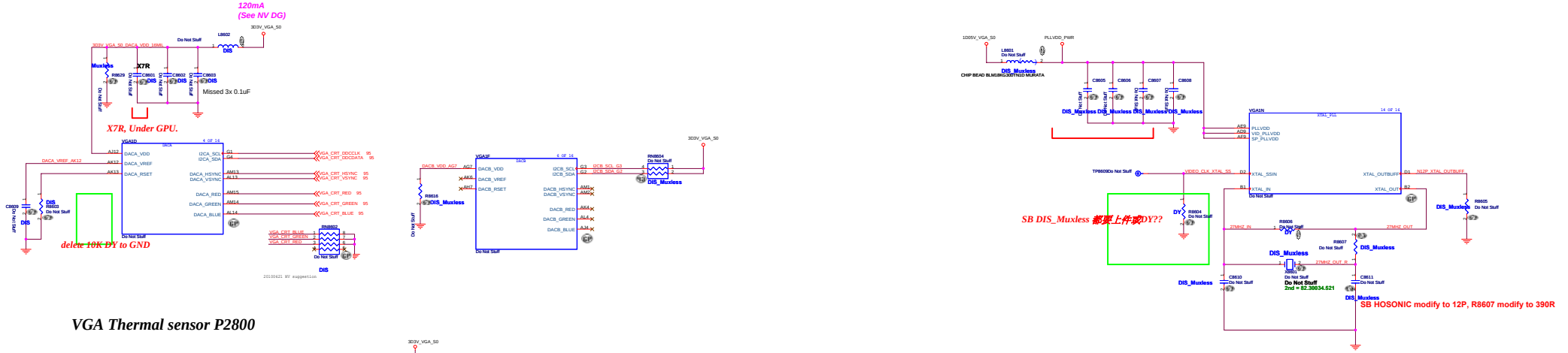
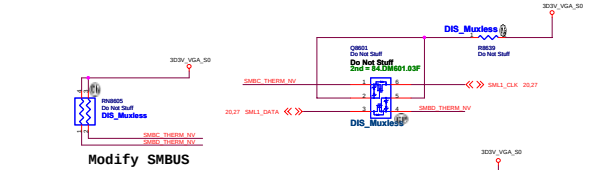
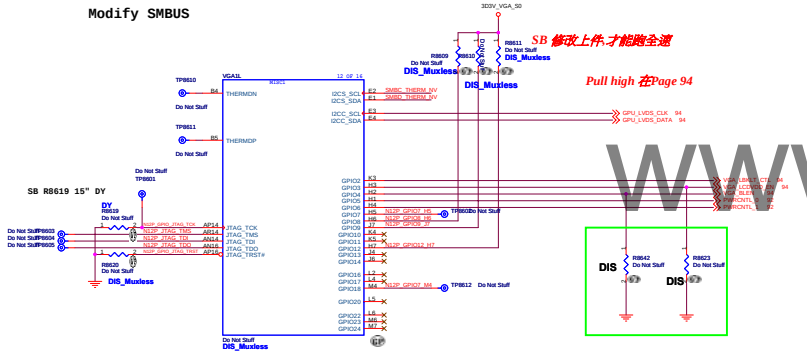
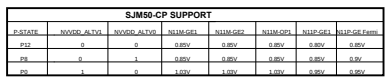
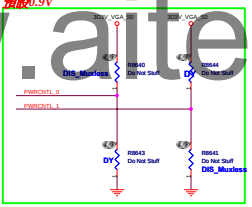


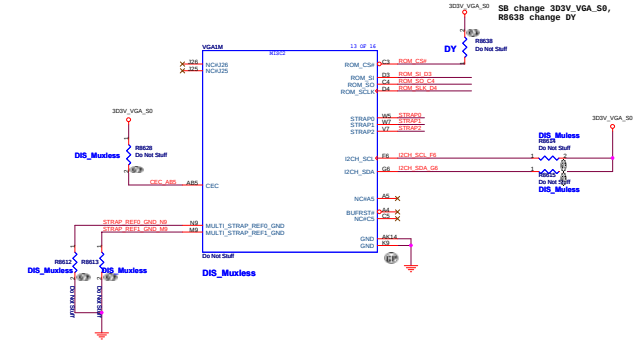
VGA Thermal sensor P2800











NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

for 1Gbit Hynix VRAM	for 2Gbit Hynix VRAM	for 1Gbit Samsung VRAM	for 2Gbit Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=0	RAM_CFG[0]=1	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=1	RAM_CFG[2]=0	RAM_CFG[2]=1
RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO

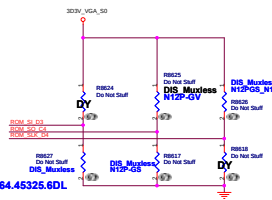
VGA_DEVICE =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417 =0 (High bit)

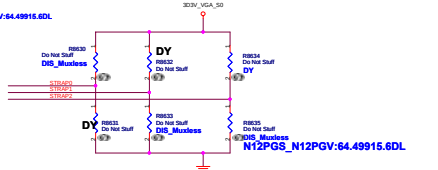
GPU_ROM_SCLK

PEX_PLL_EN_TERM =0
SLOT_CLK_CFG =1
SUB_VENDOR =0
PCI_DEVID[4] =1 N11P Fermi QS 1

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111





Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

TABLE NVIDIA 71.0N12P.E0U -1 modify N12P GV setting 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS USE 1111 (45K) — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1 — USE 0110 (35K)

STRAP2 PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)

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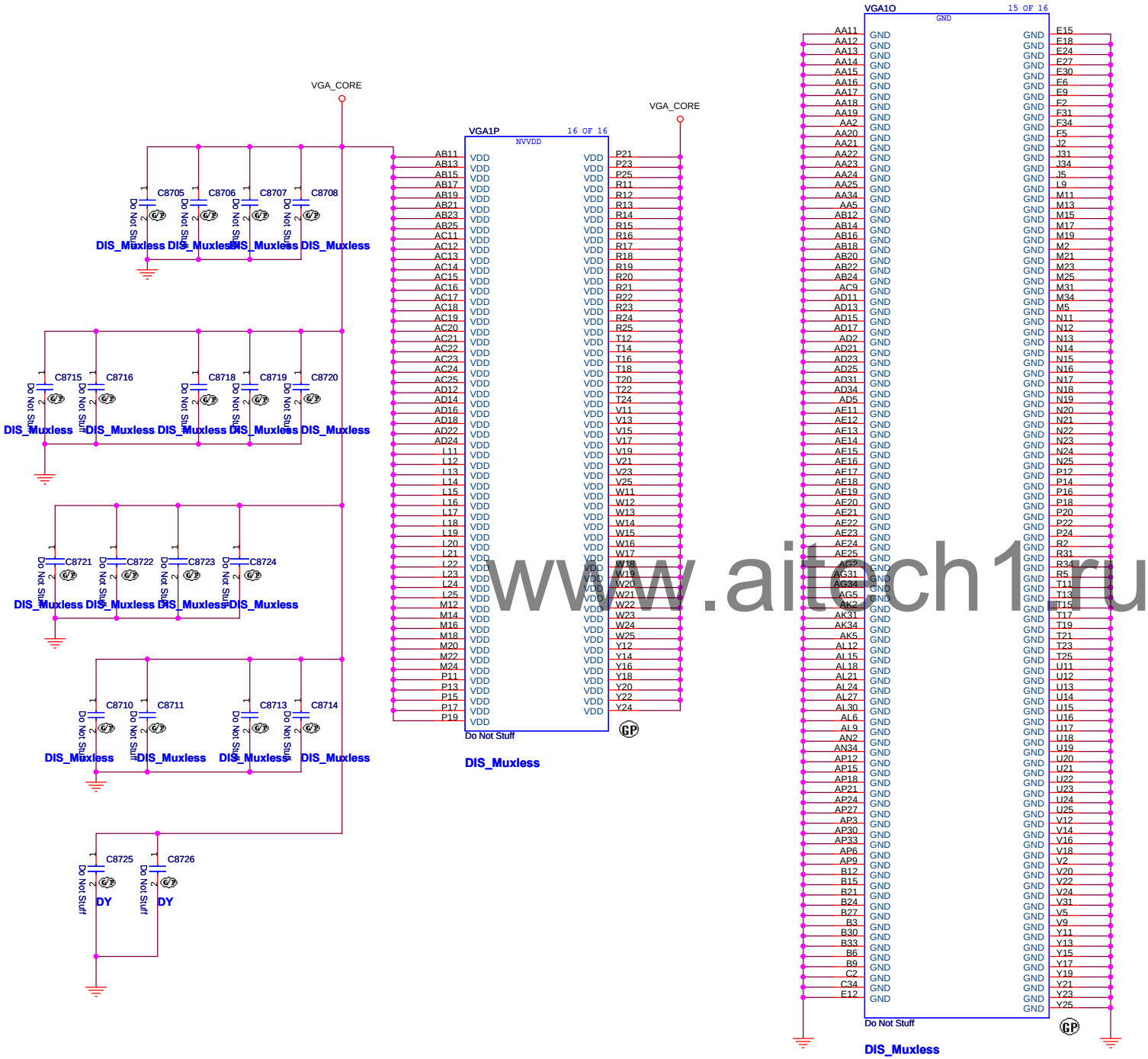

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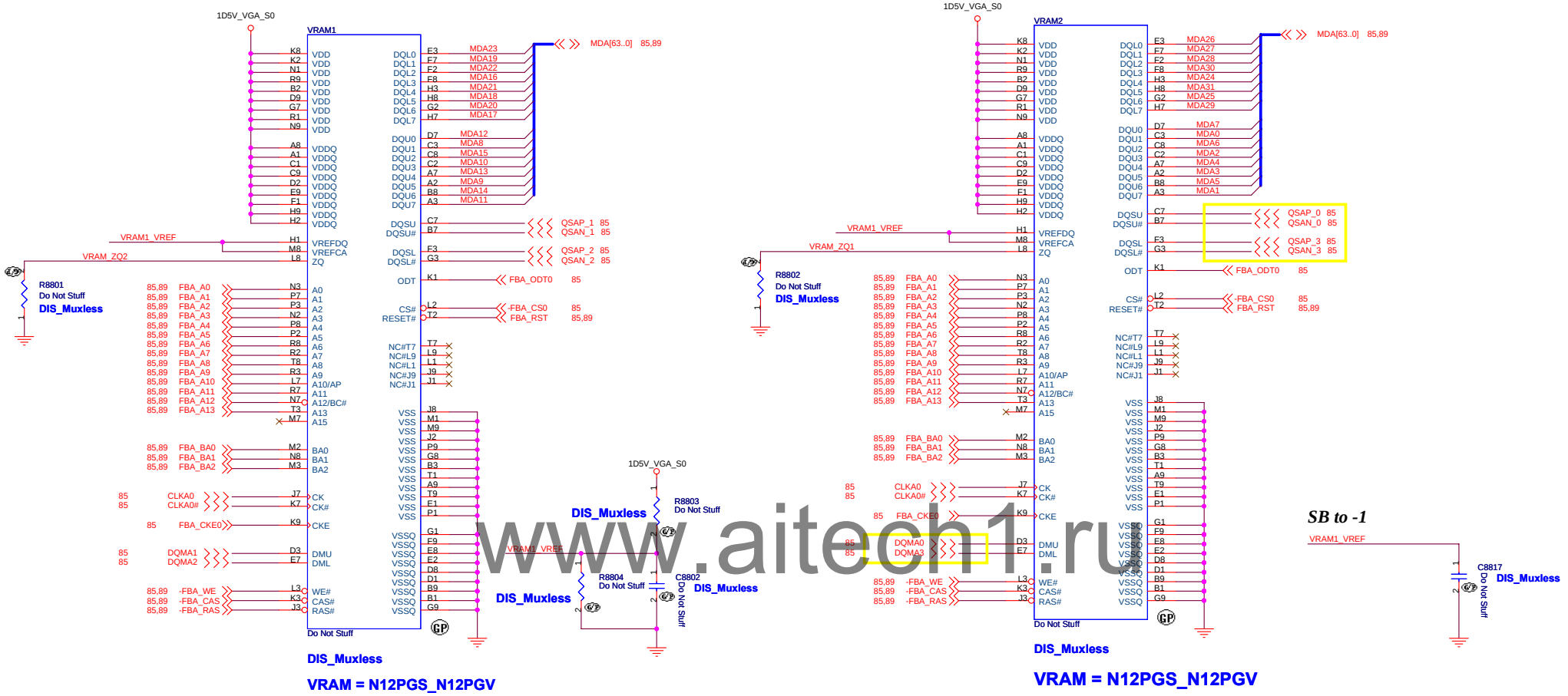

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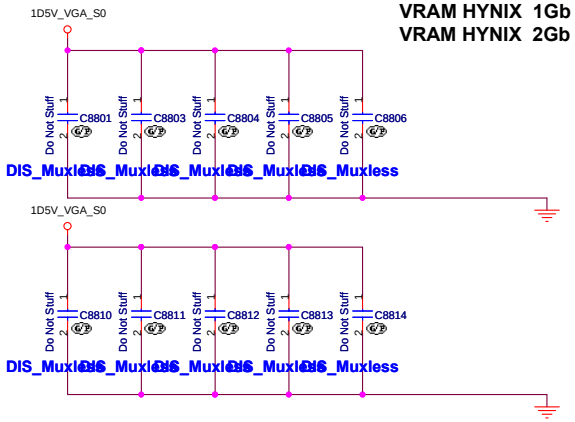
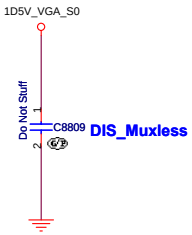
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001





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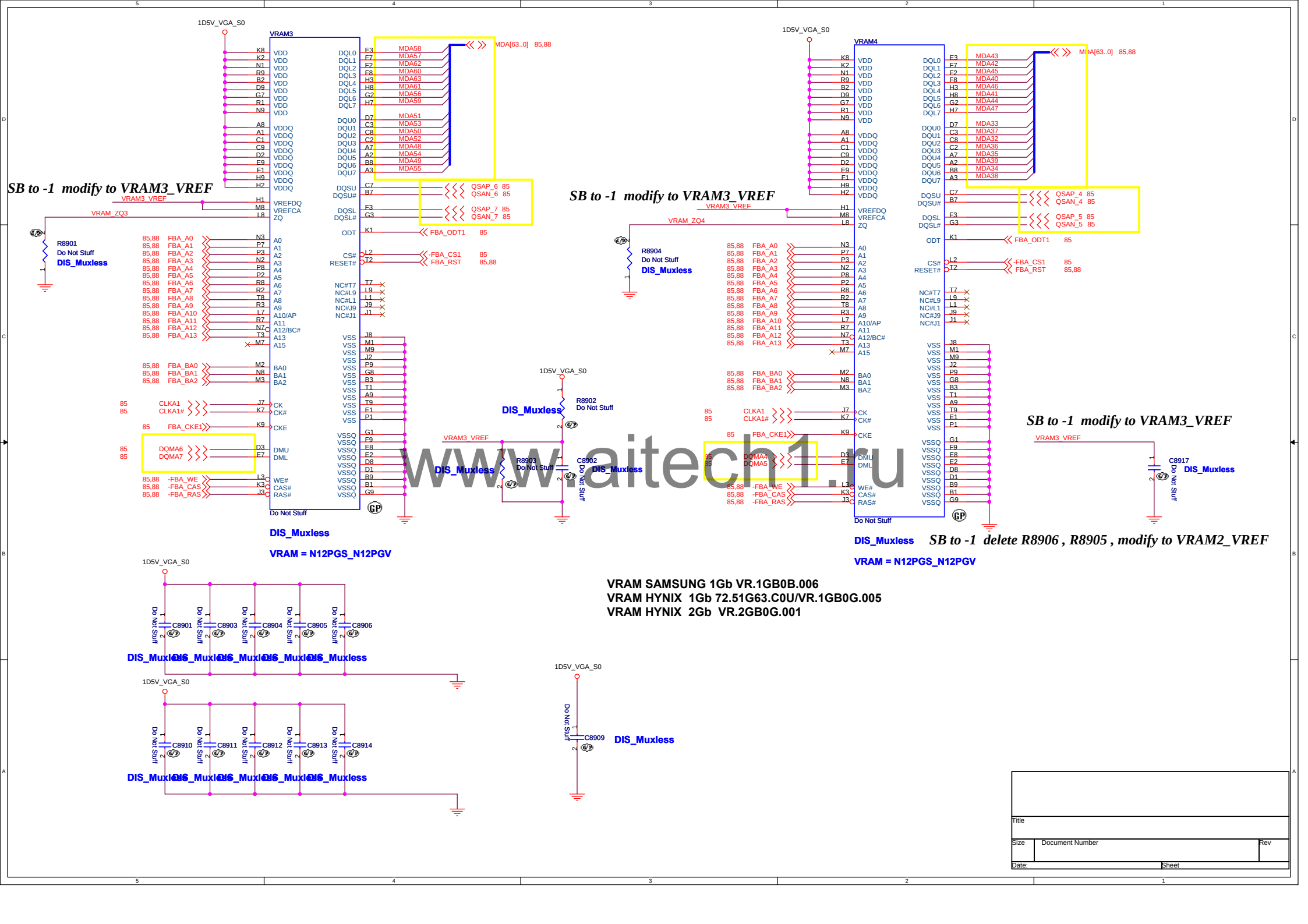

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VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
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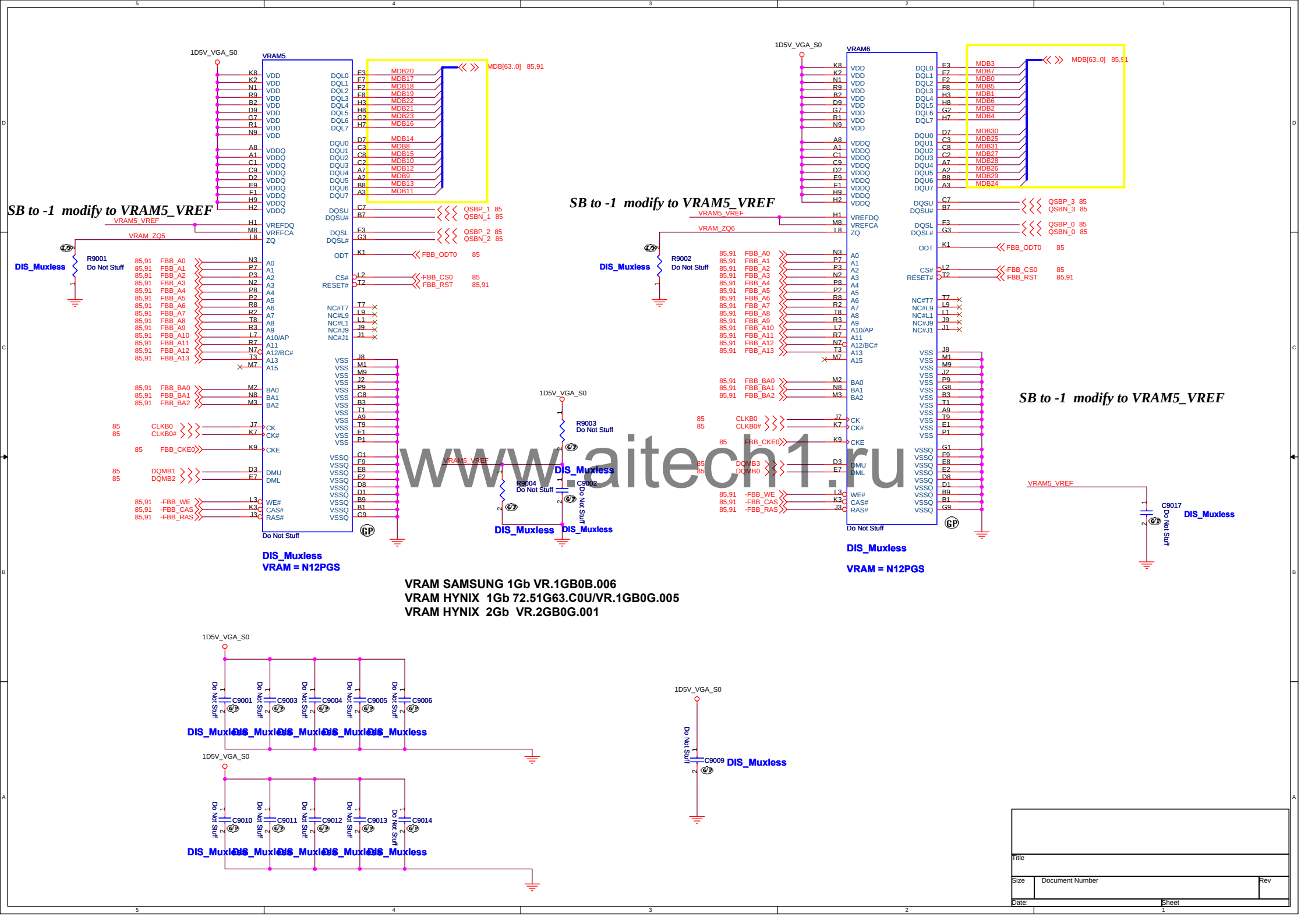

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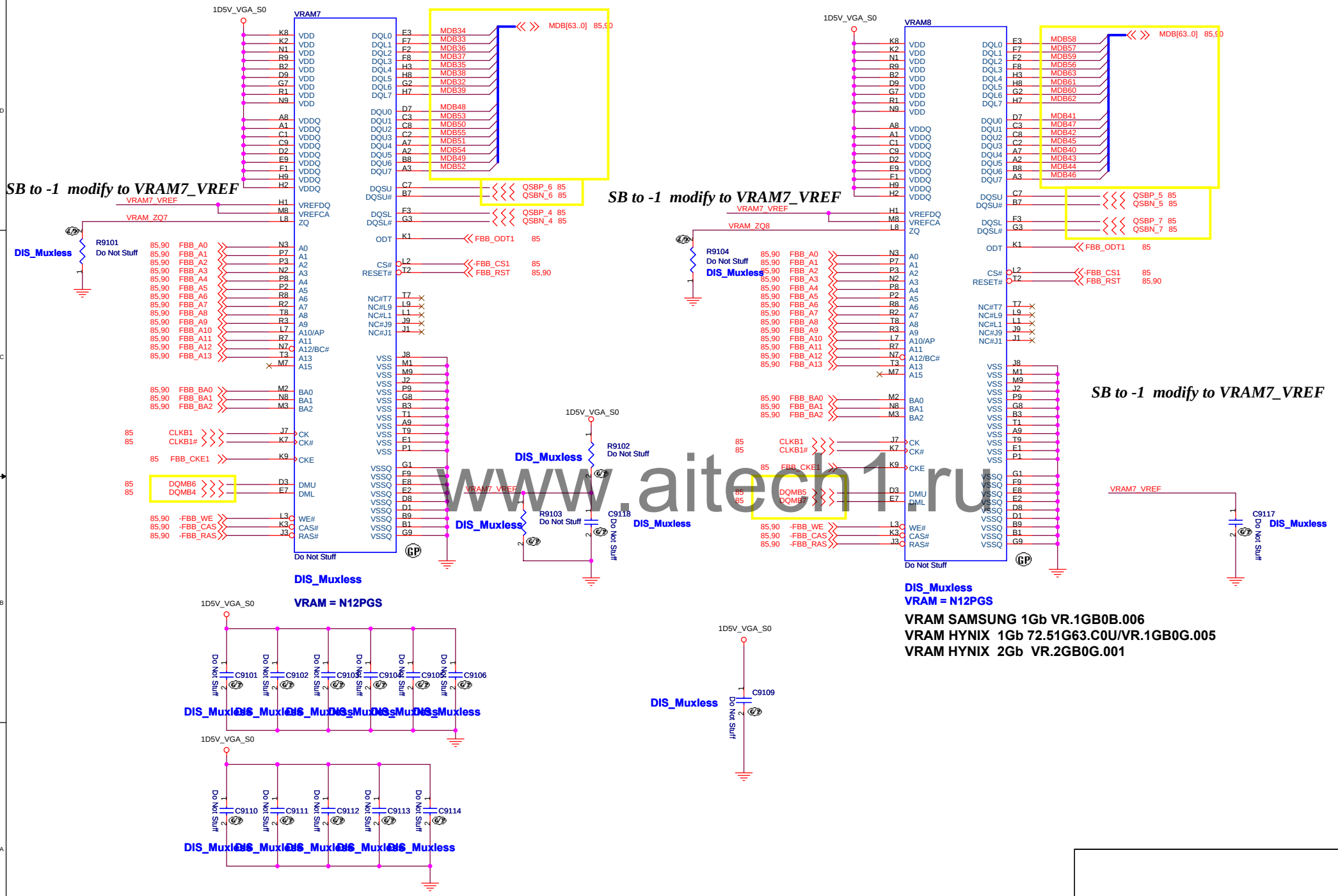

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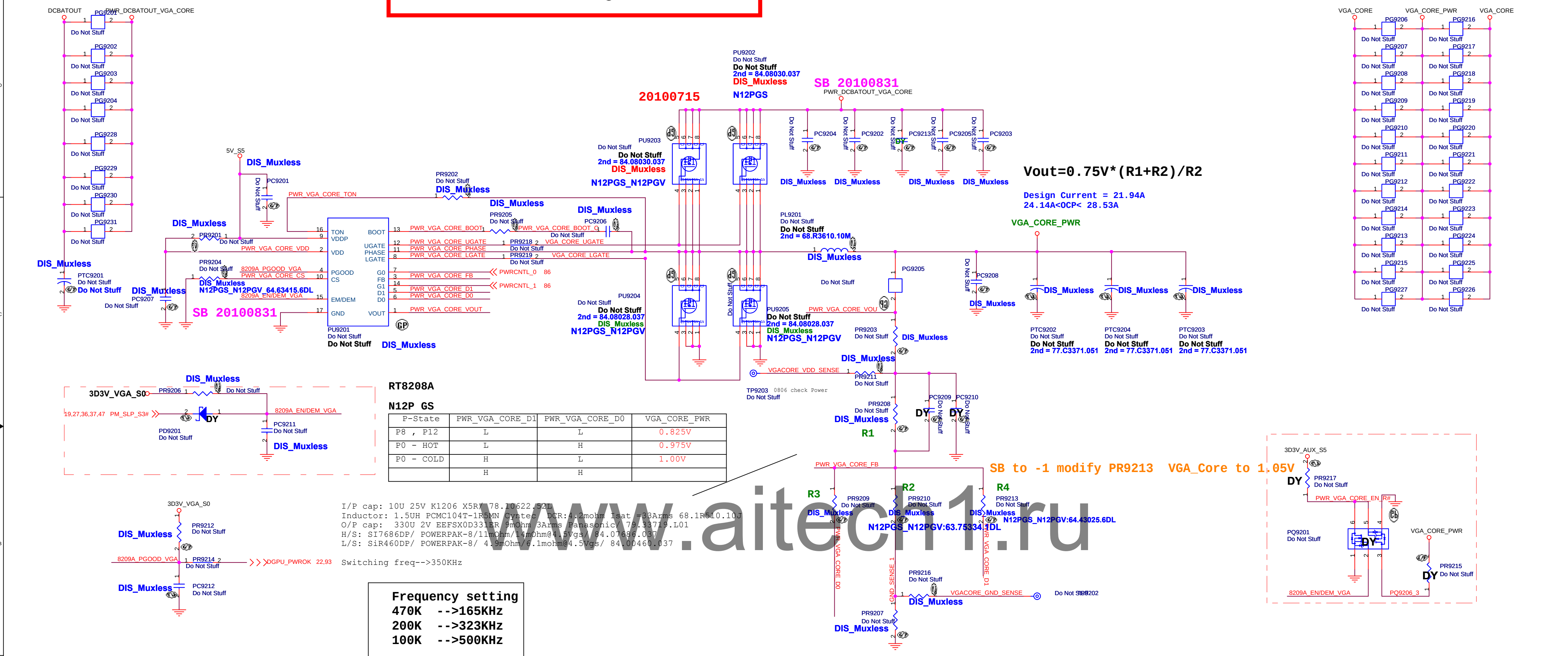
SSID = PWR.Plane.Regulator_GFX



Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

SB to -1 modify PR9213 VGA_Core to 1.05V

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

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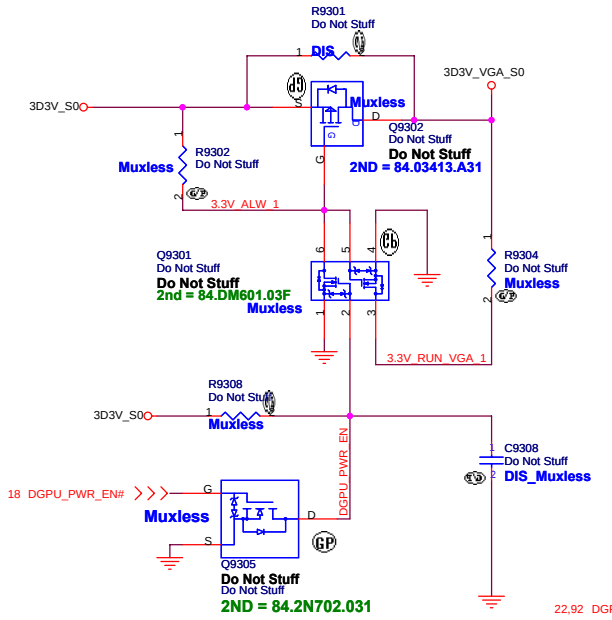
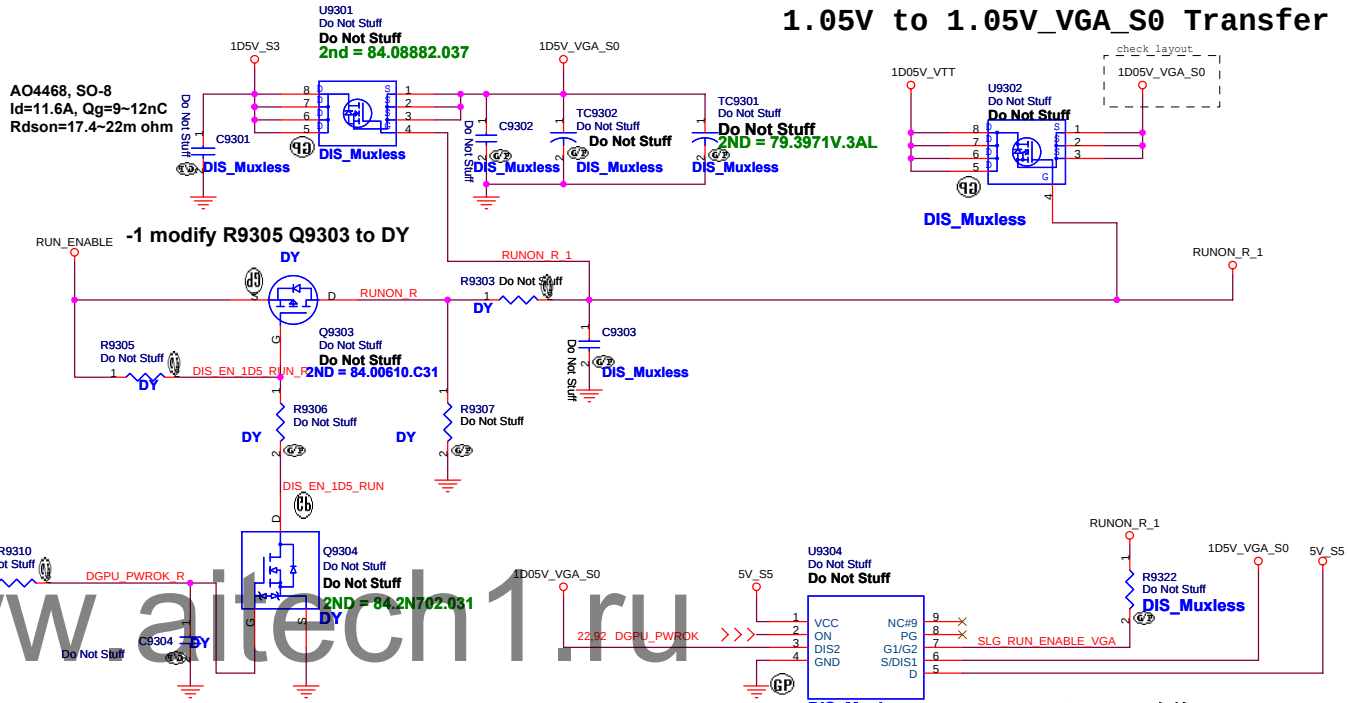
+3VS to 3.3V_DELAY Transfer



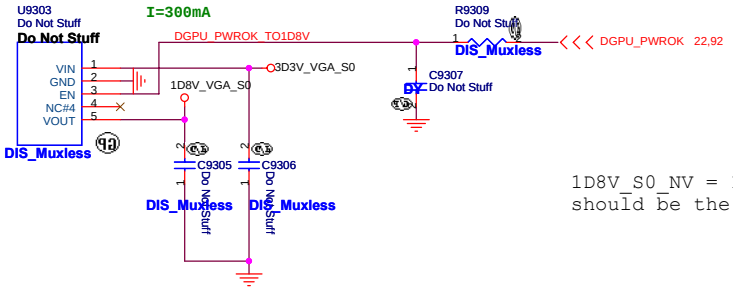
1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

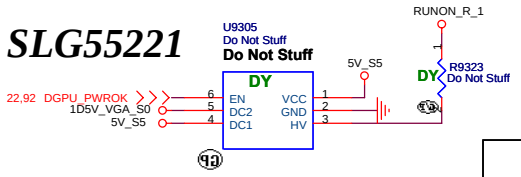


+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



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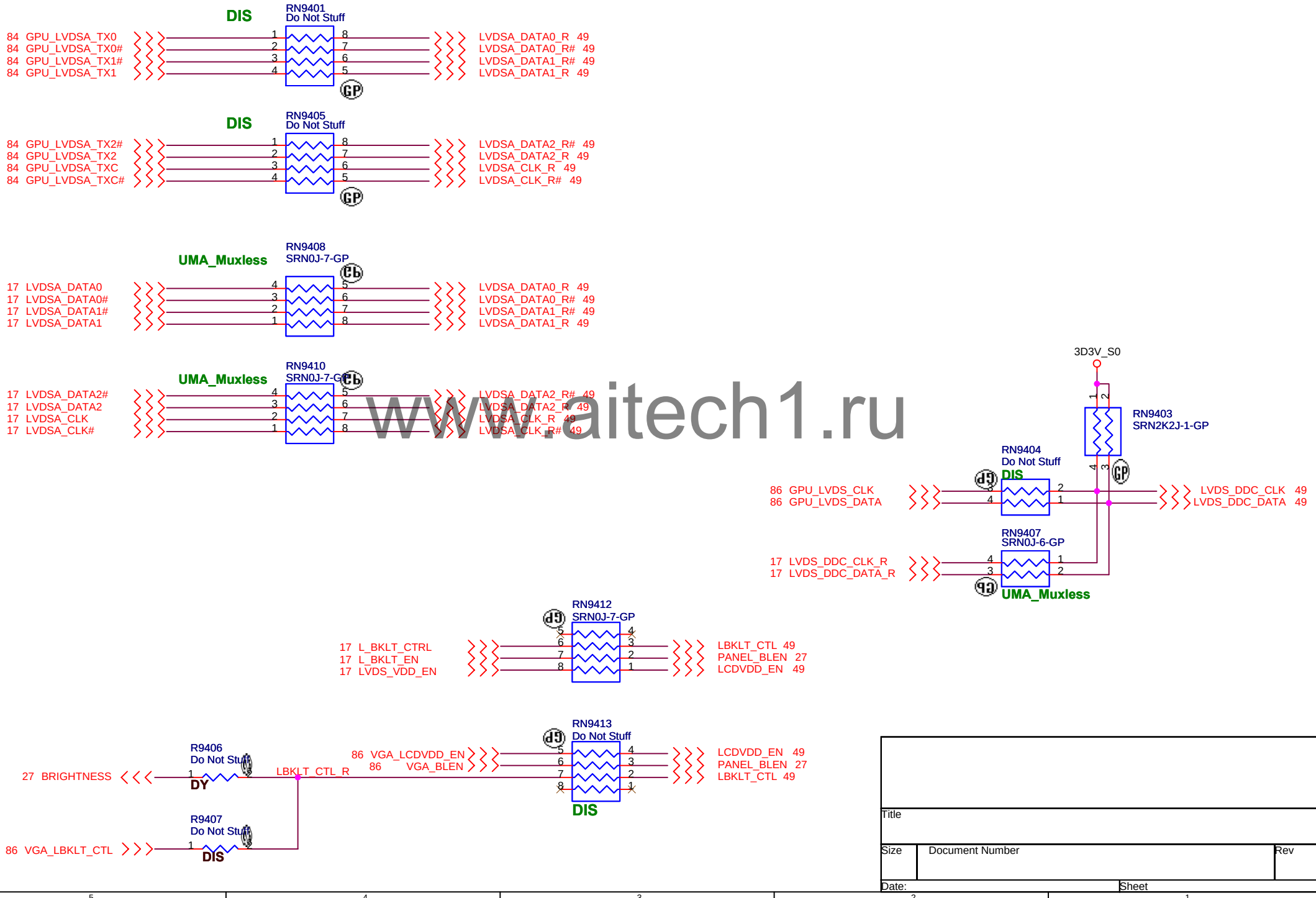

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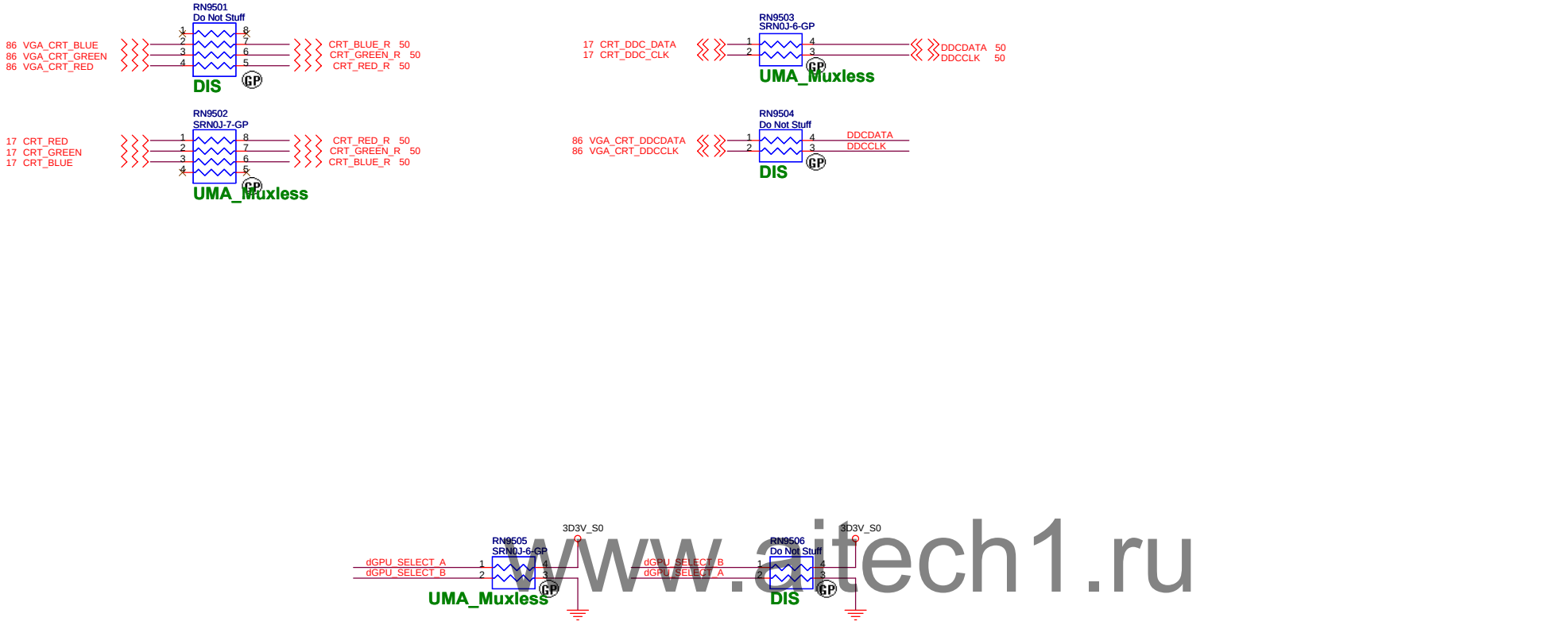

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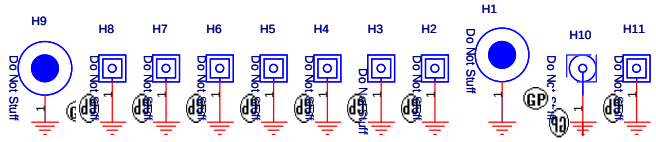
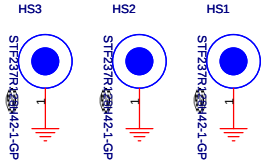
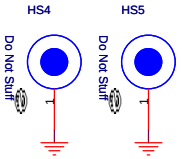


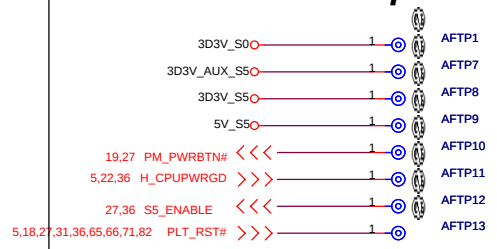
CPU



VGA



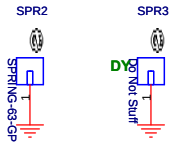
Check test point



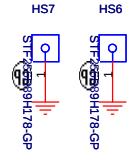
Test Point放在Dimm Door打開可量測處

SB to -1 BOM add SPR2

-2 delete SPR5



Change:34.40V16.001



3G Sku

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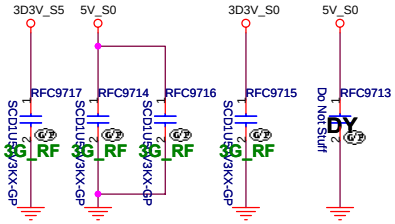

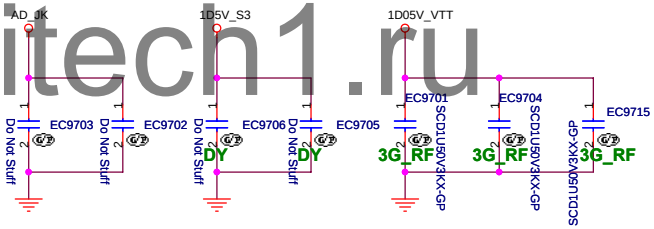

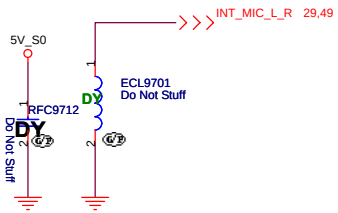

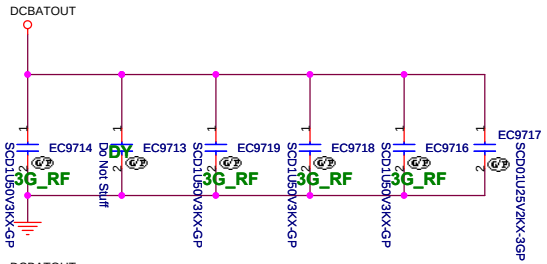

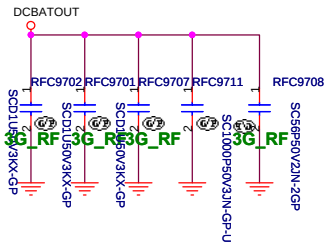

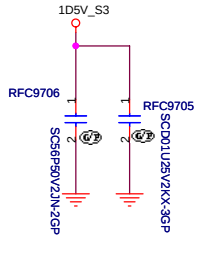

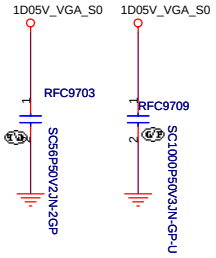

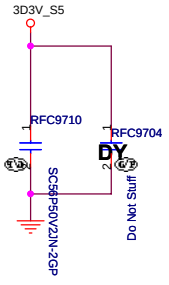

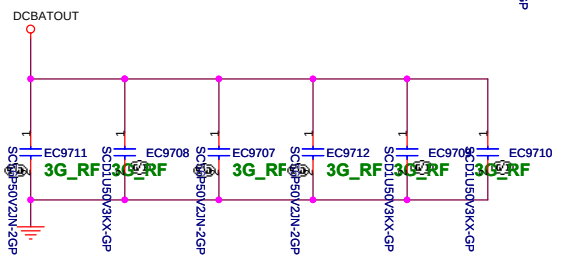

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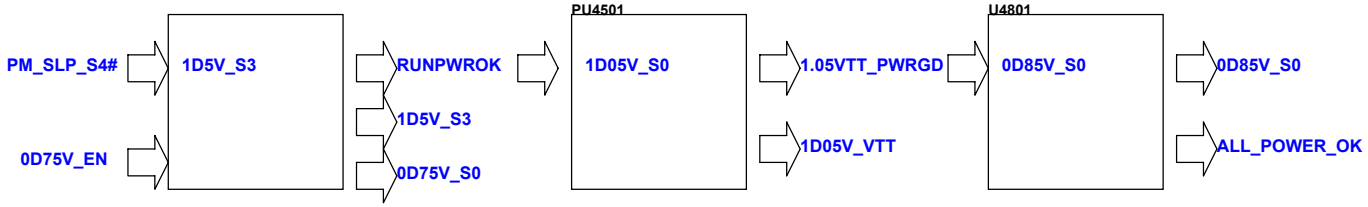

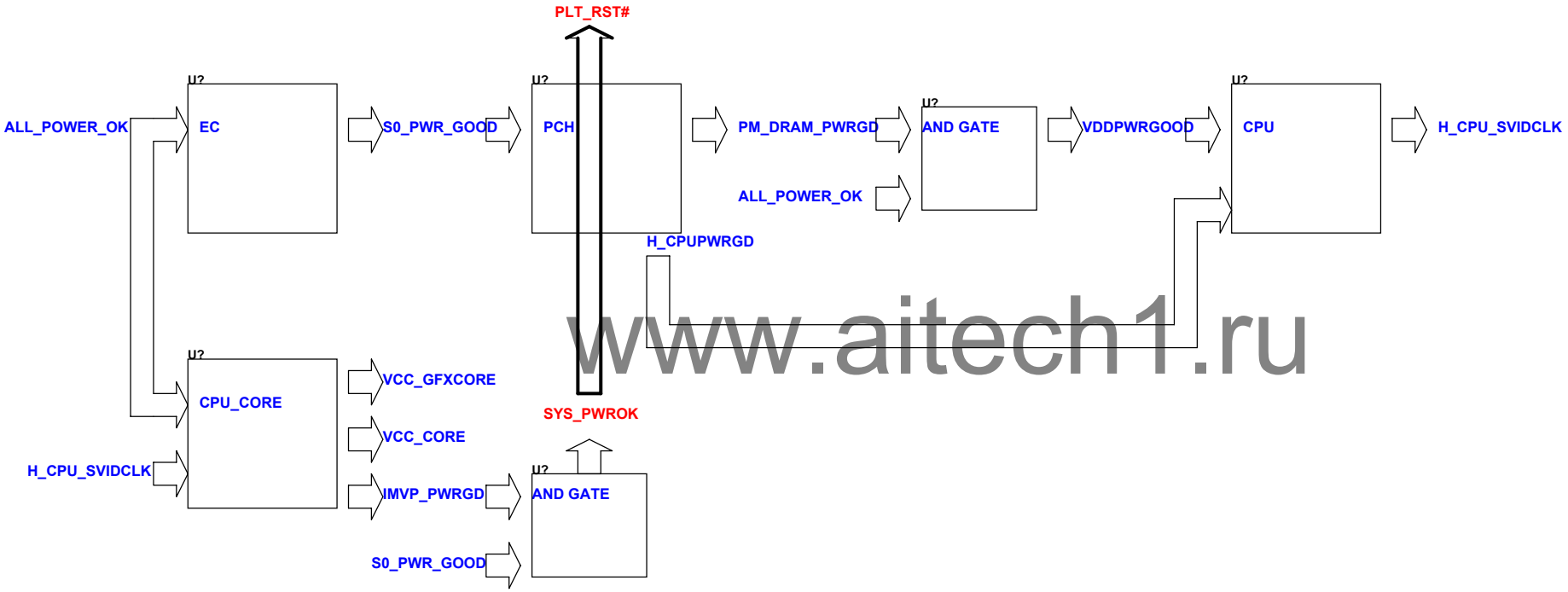

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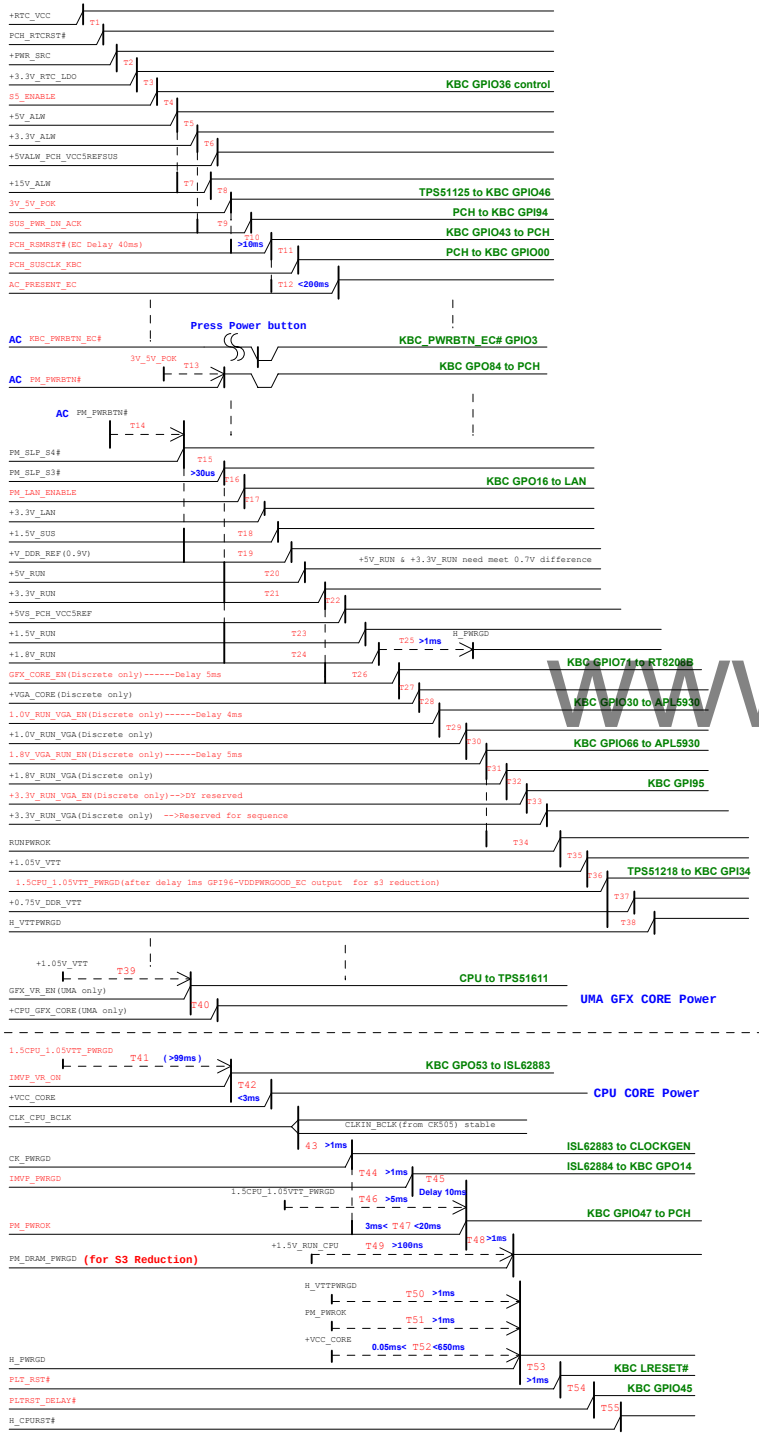
Intel-Power Up Sequence

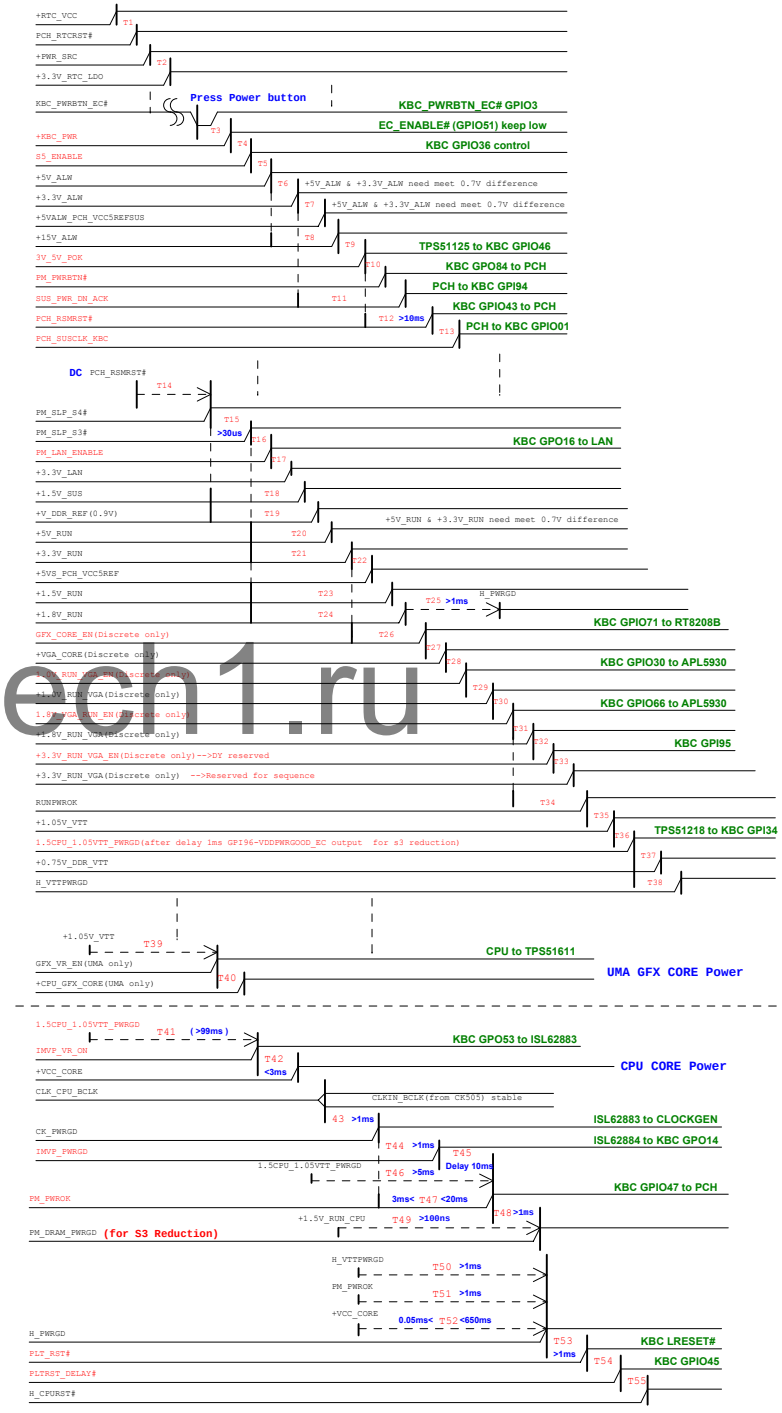
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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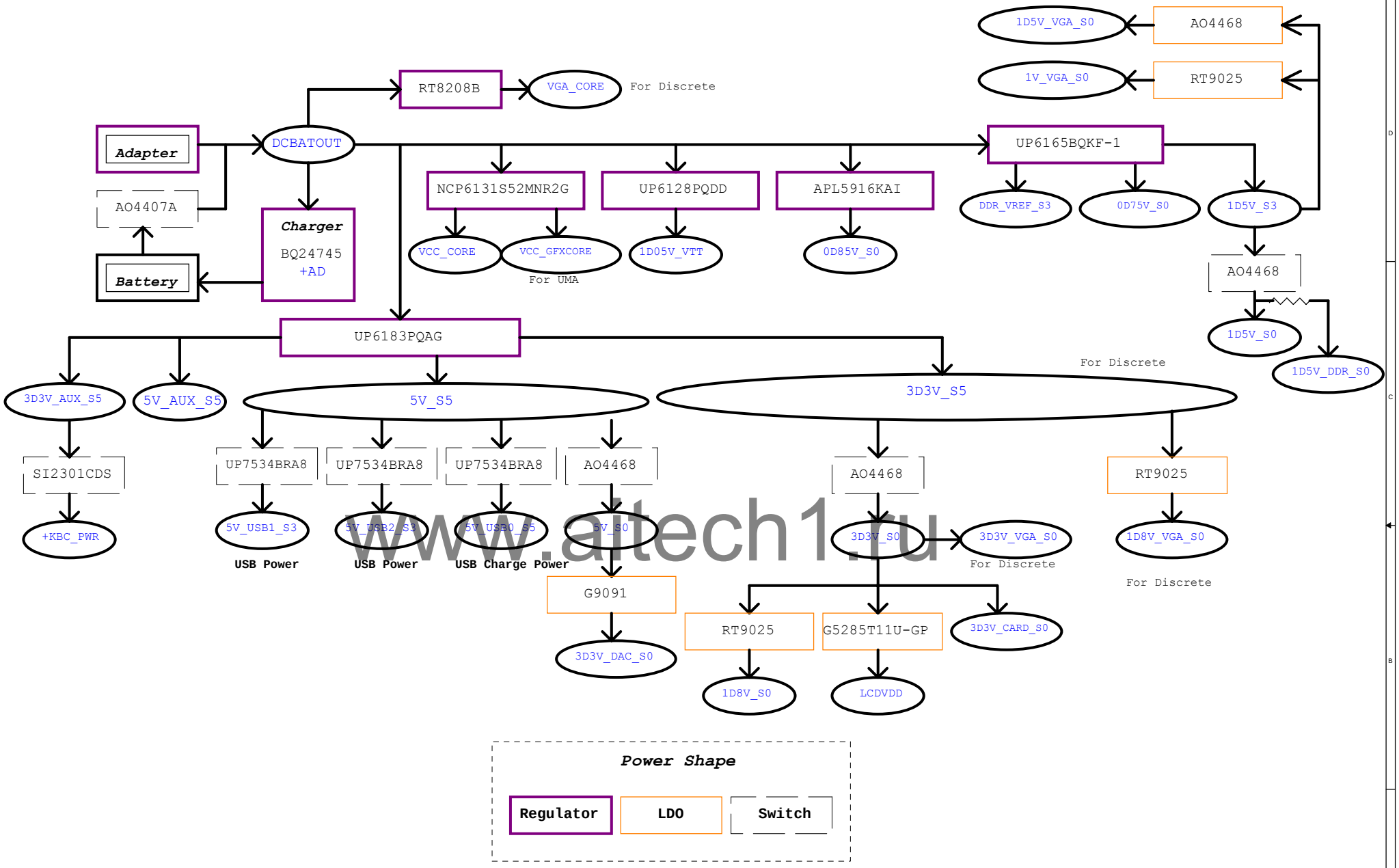

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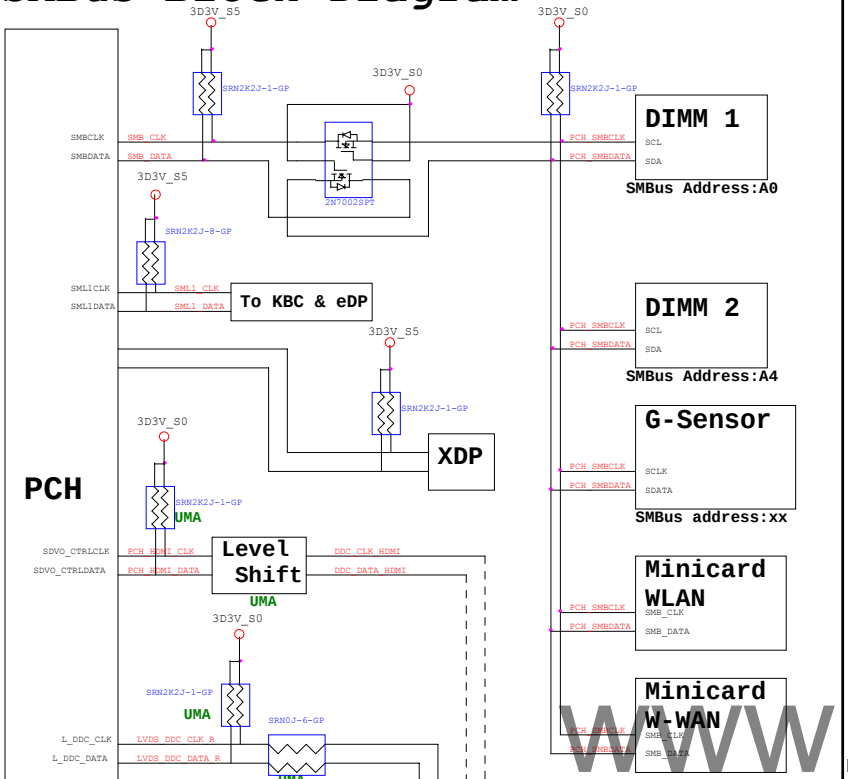
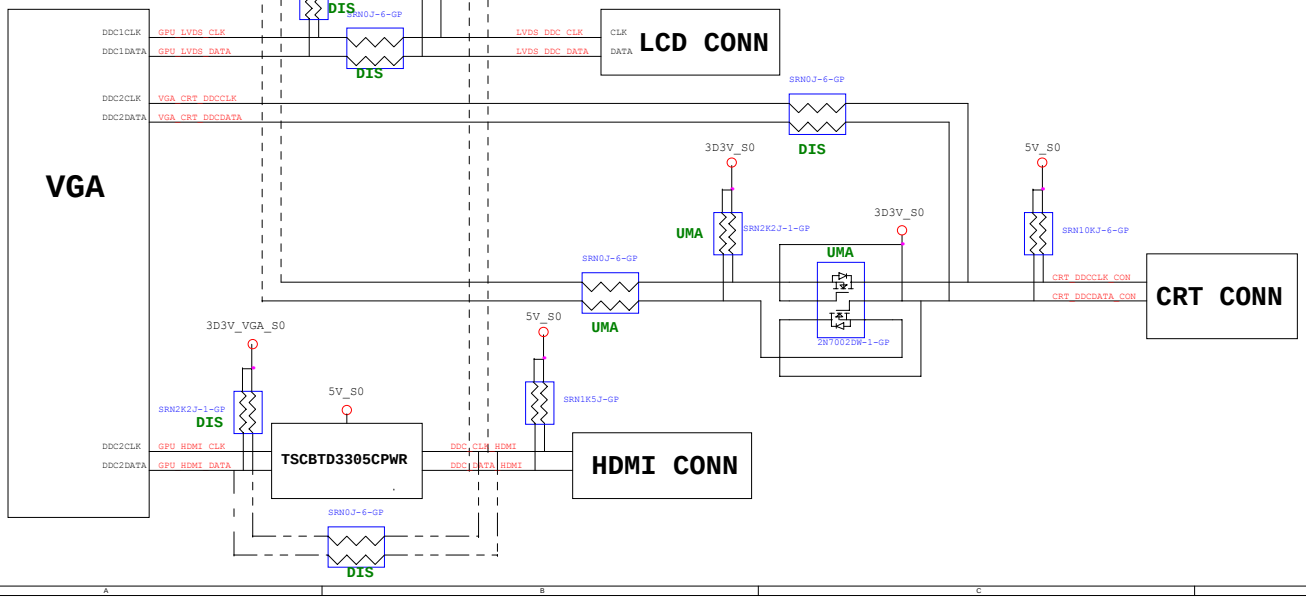
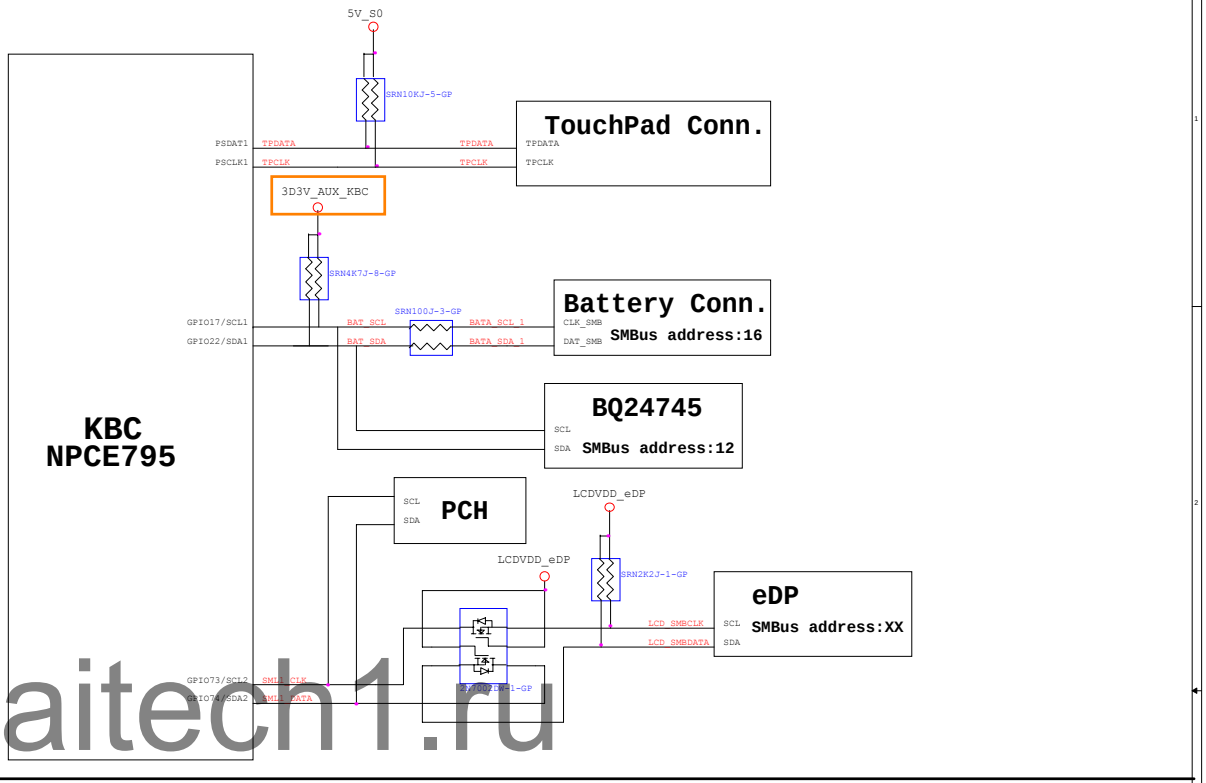
PCH SMBus Block Diagram





KBC SMBus Block Diagram



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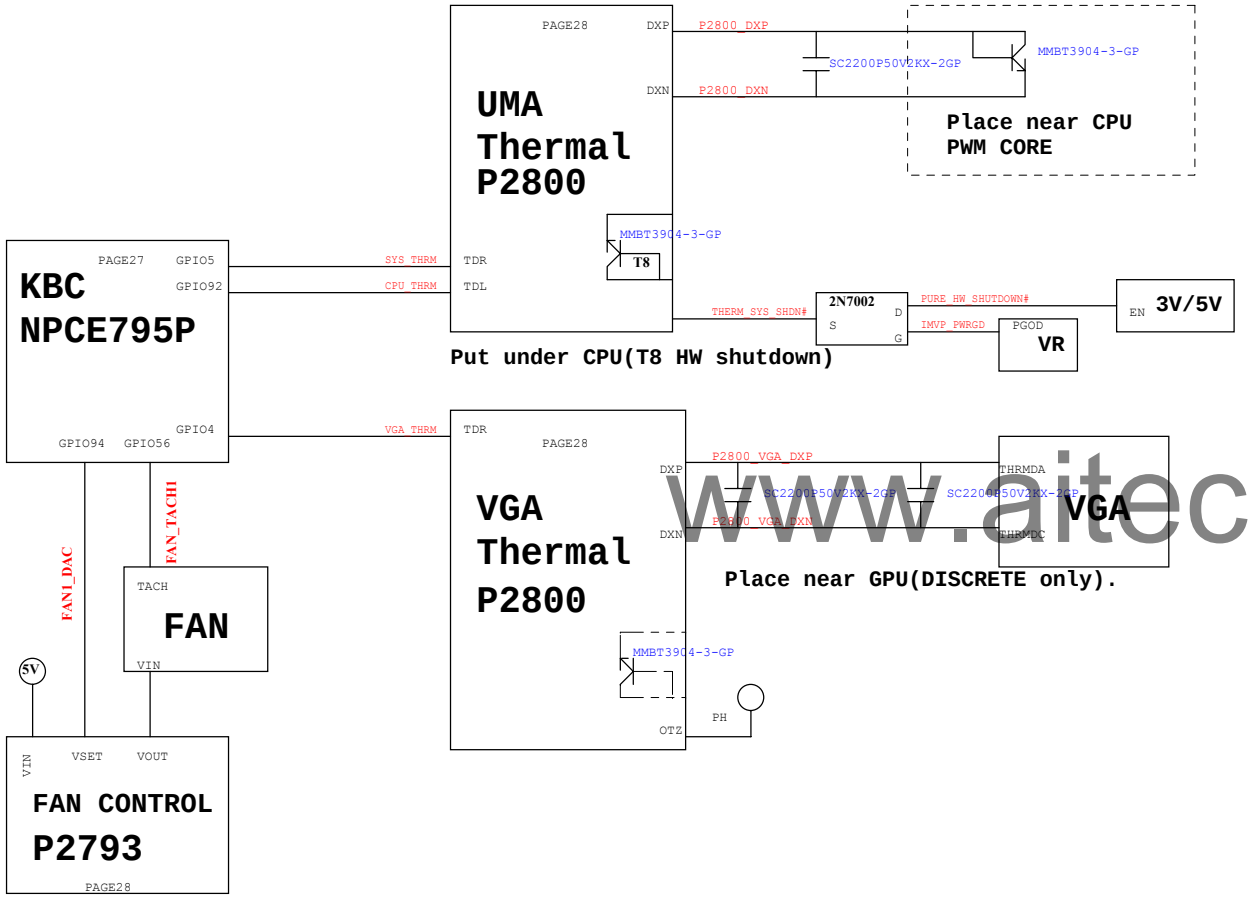
Thermal Block Diagram



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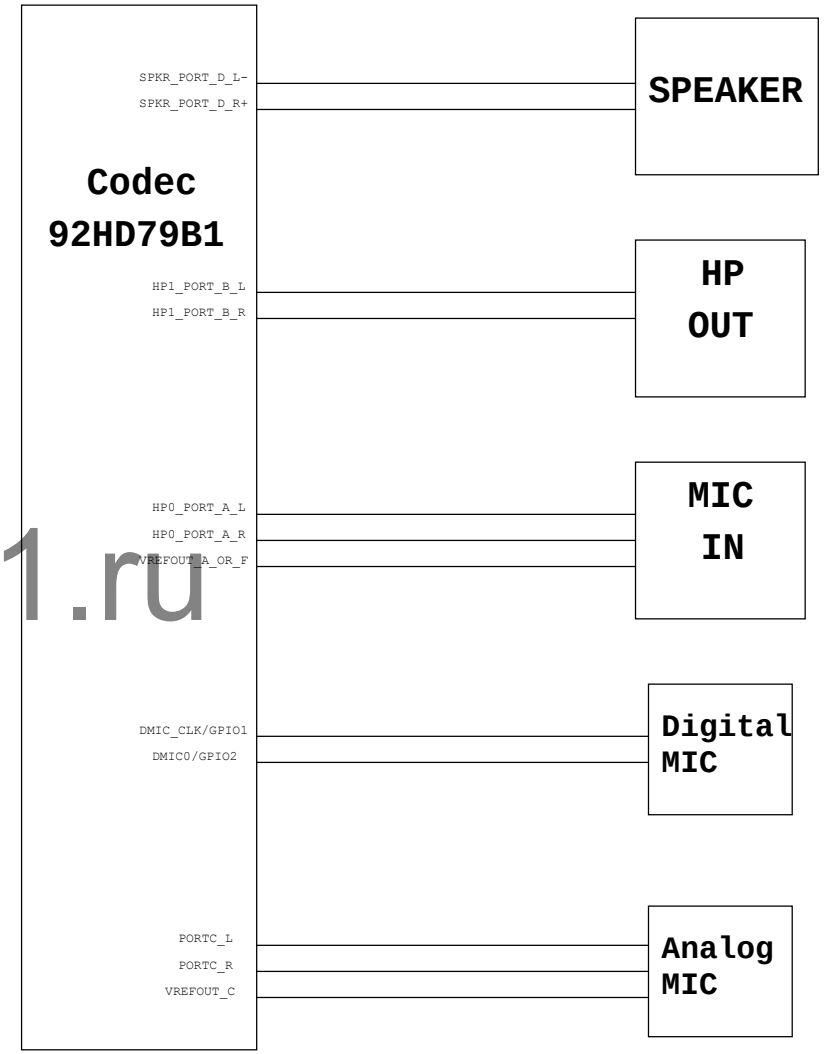
Audio Block Diagram



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